DANA.

Instruction Manual

980444

MODEL 5333 DIGITAL MULTIMETER

Publication
980444

PRELIMINARY MANUAL

MODEL 5333

DIGITAL MULTIMETER

5333/703-S-4283

This manual is to be used in conjunction with either the 603 or 703 Signal Conditioning Module manual.

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February 1971

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SECTION 1

INTRODUCTION

1.1 SCOPE.

1.2 This manual describes the Model 5333 Digital Multimeter. Descriptions are limited to the mainframe assembly which includes the digital and display module, power supply, and BCD Output module. The Signal Conditioning section of each instrument is covered in a separate manual: Model 603 or Model 703 Signal Conditioning Modules manuals.

1.3 MECHANICAL DESCRIPTION.

1.4 Model 5333 is a thin-line instrument (3-1/2 inches high) designed for standard rack mounting. The Digital and Display Module, comprising the left-hand portion of Model 5333 contains the actual measurement circuits of the DMM.

1.5 The Power Supply Module, located at the rear of the instrument, provides all the DC voltages needed by the machine and serves as an interconnection board for all other modules. The BCD Output Module (optional) plugs into the rear of the instrument and provides isolated 1-2-4-8 coded BCD output for use in data systems.

1.6 The output is displayed on a five-digit visual display with a sixth over-range digit that extends full-scale of each range by 20% (99999 to 119999). Auto-

matic ranging is performed by internal circuits which determine the optimum range and switch to that range automatically.

1.7 ELECTRICAL DESCRIPTION.

1.8 The Digital and Display module (figure 1.2) measures the analog voltage from the Signal Conditioning Module by the high-accuracy dual-slope integration technique. The amplitude of the signal is measured by comparing it to a highly stable internal reference voltage. The DMM readout displays the contents of a counter which measures the time required for the integrator voltage to change from the level of the input signal to zero. The value displayed is equal to the voltage level of the input. A new reading is taken every 300 milliseconds with the OFF-ON-HOLD switch in the ON position. The HOLD position permits the instrument to remain at the last reading indefinitely. Reading accuracy of the DMM is maintained through the use of a highly stable, zener-regulated, internal reference voltage.

1.9 SPECIFICATIONS.

1.10 Specifications are listed in table 1.1.

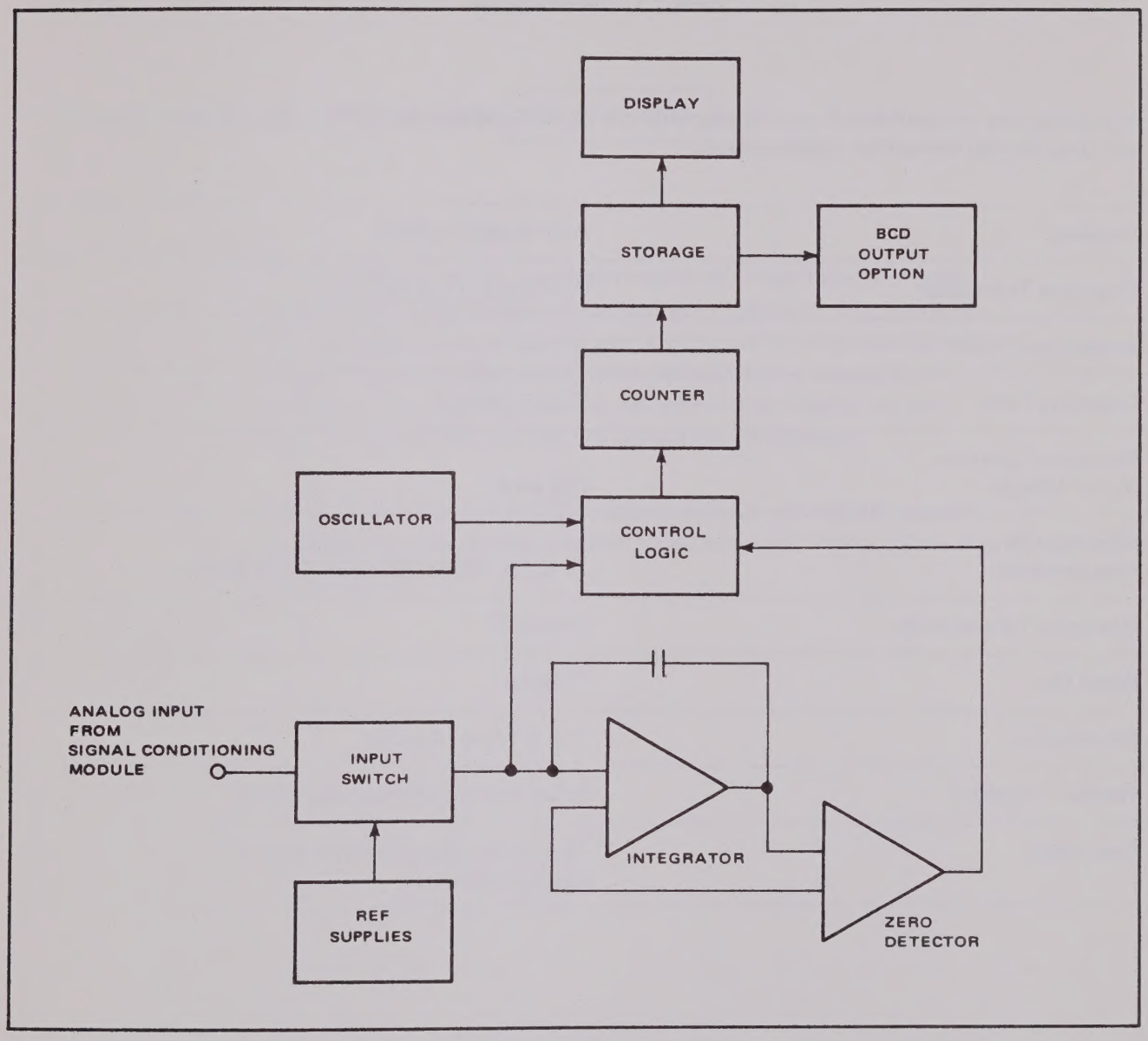


Figure 1.2 - Block Diagram

Table 1.1 - Specifications

(Specifications for individual functions vary with the Signal Conditioning module. See the appropriate Signal Conditioning manual for specifications.

Ranging:	Automatic or manual
Digitizing Technique:	Dual Slope Integrator
Integration Time:	100 ms
Digitizing Time:	220 ms max.
Maximum Common Mode Voltage:	250 volts
Maximum Power Requirements:	25 watts, 105 to 125 volts, 50 to 400 Hz
Operating Temperature:	0 to 50°C
Warm Up:	1/2 hour
Dimensions:	17 x 3-1/2 x 14 inches
Weight: (Approx)	15 pounds net, 20 pounds shipping
Guarantee:	12 months, faulty workmanship or component failure

SPECIAL NOTE

The shipping carton and its internal support structure have been scientifically designed for maximum protection of the instrument. Dana recommends saving the carton and contents for use in future reshipping of the instrument. Alternate packing methods, such as plastic foam blocks and loose packing material, may prove to be insufficient for maximum protection and result in damage during shipment.

If reshipping is required and the original carton is not available, special packing instructions can be obtained from Dana Labs' Product Service Department.

SECTION 2

INSTALLATION

2.1 UNPACKING AND INSPECTION.

2.2 The DMM is sandwiched between two forms of plastic foam and packed in a double-walled cardboard carton for shipment. The plastic forms hold the DMM securely in the carton and absorbs any reasonable external shock normally encountered in transit. Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the DMM from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 The instrument, as shipped, is designed for bench-top operation. A stand-up bracket is provided under the case to aid in reading the visual display. The Model 5333 instrument can be adapted for rack installation with two flange mounting holes located in each of the two side panels. The rack-mounting kit (Dana 402588) is attached to the instrument by removing and discarding the four set screws occupying the mounting screw holes and securing the two rack-mounting flanges to the side panels of the instrument with the four screws contained in the rack-mounting kit.

2.4 POWER CONNECTIONS.

2.5 A standard eight-foot, three-wire, power cable is supplied with the instrument. This cord connects to a three-pin power connector at the rear of the unit.

NOTES

1. If the DMM has been stored for a prolonged period (5 or 6 months), without use, it is recommended that it be operated with a variable transformer, such as a Variac, at one-half line voltage for about two hours before gradually applying full power. This is done to "reform" the electrolytic capacitors in the amplifier and reduce the chance of capacitor failure.

2. To clean the glass on the readout panel, use a commercial glass cleaner such as Windex. Do not use alcohol or other cleaners containing ketones.

2.6 OPERATION.

2.7 For proper measurement connections and procedures, refer to the appropriate Signal Conditioning manual (603 or 700/703).

DANA

MANUAL CHANGES

Dana Model 5333

Publication No. 980444

Date of Publication February 1971

Date of Change August 1971

Change #1 — Paragraph 3.6, page 3-2, connector J35 should be: connector J36

Change #2 — Table 3.1, page 3-3, J35 Pin Assignments should be: J36 Pin Assignments

SECTION 3

BCD OUTPUT OPTION
(MODEL 95)

3.1 INTRODUCTION.

3.2 The isolated BCD output accessory enables the DMM to interface with either a grounded or ungrounded printer or other output device and still maintain a high level of common-mode rejection. Isolation of the guarded circuits of the DMM from external circuits is achieved through the use of optical couplers.

3.3 Optical Couplers. Each optical coupler (figure 3.1) is a MCT2 type electro-optical isolator. It consists of a light-emitting diode (LED) and a photo-transistor. The LED emits light when forward-biased. This light is transmitted through a "light pipe" to the phototransistor. In a phototransistor, base current is generated by light incident on the base-collector junction. The resulting collector current is proportional to the forward-bias current applied to the LED.

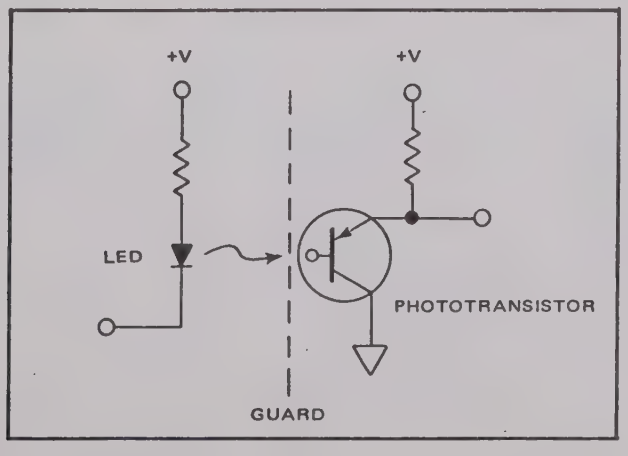


Figure 3.1 - Photo Coupler

3.4 In the DMM, a command at the BCD output connector forward-biases the LED. Figure 3.2 shows a typical program input line. The typical command, $\overline{X}$, is inverted twice and applied to the anode of the LED. The resulting collector current of the phototransistor produces a $\overline{X}$ at the input of the TTL command logic.

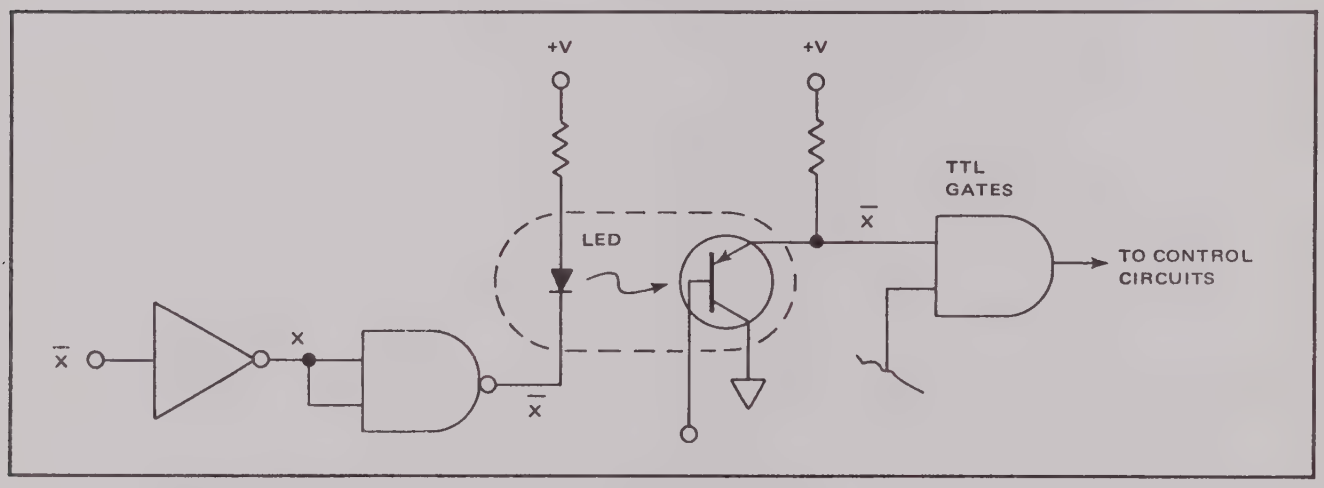


Figure 3.2 - Typical BCD Output Circuit

3.5 BCD OUTPUTS.

3.6 All output data is delivered through the BCD Output connector J35 on the rear panel. Outputs are positive true at TTL logic levels (0 to +0.4 volts, false; +2.4 to +5.0 volts, true). Pin assignments are listed in table 3.1. Voltage levels are referenced to common, pin 24. Numerical output data lines are identified in table 3.1 by decade and BCD weight. Codes for all outputs are described in the following paragraphs.

Table 3.1 - J35 Pin Assignments

	Pin No.		
Range 1	1	26	Range 4
Range 2	2	27	Range 8
Polarity 1	3	28	Polarity 4
Polarity 2	4	29	Polarity 8
Units 1	5	30	Units 4
Units 2	6	31	Units 8
10's 1	7	32	10's 4
10's 2	8	33	10's 8
100's 1	9	34	100's 4
100's 2	10	35	100's 8
1000's 1	11	36	1000's 4
1000's 2	12	37	1000's 8
10,000's 1	13	38	10,000's 4
10,000's 2	14	39	10,000's 8
100,000's 1	15	40	100,000's 4
100,000's 2	16	41	100,000's 8
Function 1	17	42	Function 4
Function 2	18	43	Function 8
Not Used	19	44	Not Used
Not Used	20	45	Not Used
Overload	21	46	Not Used
$\overline{\text{Delayed Command}}$	22	47	$\overline{\text{Hold}}$
$\overline{\text{Direct Command}}$	23	48	$\overline{\text{Print}}$
$\overline{\text{Common}}$	24	49	$\overline{\text{Superfast}}$
Ext. Accessory Volt.	25	50	5-Volt Ref.

3.7 Function Codes. Codes for function outputs are listed below:

Function	Pin 17 F1	Pin 18 F2	Pin 42 F4	Pin 43 F8
DC	0	0	0	0
DC Filtered	0	0	1	0
AC	1	0	0	0
Ohms	0	1	0	0
Ohms Filtered	0	1	1	0
DC Ratio	0	0	0	1
DC Ratio Filtered	0	0	1	1

3.8 Range Codes. Codes for range outputs are listed below:

Range	Pin 1 R1	Pin 2 R2	Pin 26 R4	Pin 27 R8
.1	0	0	0	0
1	1	0	0	0
10	0	1	0	0
100	1	1	0	0
1000	0	0	1	0
10000	1	0	1	0

3.9 Polarity Codes. Codes for polarity outputs are listed below:

Polarity	Pin 3 P1	Pin 4 P2	Pin 28 P3	Pin 29 P4
+	1	0	0	0
-	0	0	0	0

3.10 Overload. The Overload line, pin 21, is true to indicate that the magnitude of the input exceeds the maximum limits of the selected range, including overrange.

3.11 Print Command. The $\overline{\text{PRINT}}$ line, pin 48, signifies the end of the measurement cycle on its negative-going edge. The line is true during the measurement cycle and during any timeout period. $\overline{\text{PRINT}}$ indicates to the printer that the data at the output connector is available for recording.

3.12 The Hold mode is selected by a command to pin 47, $\overline{\text{HOLD}}$. Each reading is held and no new measurement made until commanded by either $\overline{\text{DIRECT COMMAND}}$ (pin 23) or $\overline{\text{DELAYED COMMAND}}$ (pin 22).

3.13 A command to pin 49, $\overline{\text{SUPERFAST}}$, selects a high-speed mode of operation (100 reading per second). In this mode, the DMM functions as a three-digit instrument with some degradation of accuracy.

3.14 A voltage of +5 volts is available at pin 50 for use as a reference level only.

3.15 READ COMMANDS.

3.16 Two command lines are provided: $\overline{\text{DIRECT COMMAND}}$, pin 23, and $\overline{\text{DELAYED COMMAND}}$, pin 22. The commands are used with the DVM in the Hold mode. A command is generated by a contact closure from the selected command line and common or a conducting transistor switch between the line and common.

3.17 A command to pin 23 initiates a new reading immediately. A command to pin 22 results in a reading after a timeout period to allow for settling of the input signal. The timeout periods vary with function and are listed in table 3.2.

Table 3.2 - Delayed Command Timeouts

Function	Timeout
DC	50 ms
DC Filtered	500 ms
AC	500 ms
OHMS	50 ms
OHMS Filtered	500 ms
DC Ratio (option)	50 ms
DC Ratio Filtered (option)	500 ms

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION.

4.2 The Digital and Display Module is a complete DC digital voltmeter. The module displays the voltage and polarity of any DC input signal between zero and 12V full-scale (including overrange). A 10V input signal gives a displayed reading of 100,000. The Digital and Display Module includes some analog circuitry and the digital circuitry. In addition, solid state switches at the the input to the Integrator are switched by the digital circuitry but perform an analog function.

4.3 Decimal points are placed by the ranging logic which is located on the Signal Conditioning Module. The driver transistors that actually switch the decimal points are located on the Digitizing and Display Module. Their driving signal, however, comes from the ranging logic on the Signal Conditioning Module.

4.4 The analog circuitry is entirely constructed around monolithic, linear, differential amplifier, integrated-circuits, which are connected either as inverting operational, or non-inverting potentiometric amplifiers. The solid-state switching circuitry, at the input to the integrator, consists of four N-channel field effect junction transistors. They and their associated driving circuitry

comprise the only other section of the Digitizing and Display Module constructed from discrete components. The Digitizing and Display Module may be broken up into the following sub-sections:

a. Analog

Reference supplies
Integrator
Null Detector

b. Digital

Clock oscillator
Counter-readout
Ranging logic
Polarity sensing logic

c. Switching Circuitry

NOTE: Individual circuits are described followed by an over-all description of operation.

4.5 REFERENCE SUPPLIES.

4.6 The reference supplies, shown in figure 4.1, are built around two types of 301A differential amplifier IC's. The primary reference supply is the +10 volt supply. The negative supply inverts the +10V supply to -10V using an operational amplifier.

4.7 The stability of the +10V reference supply is dependent upon the inherent stability of the reference zener. These zeners are individually graded by Dana to obtain maximum long term stability and minimum temperature coefficient (TC). The zener and the series resistor through which it is biased are connected across a precision 10V source. The series resistor is then factory selected (FSV) to obtain

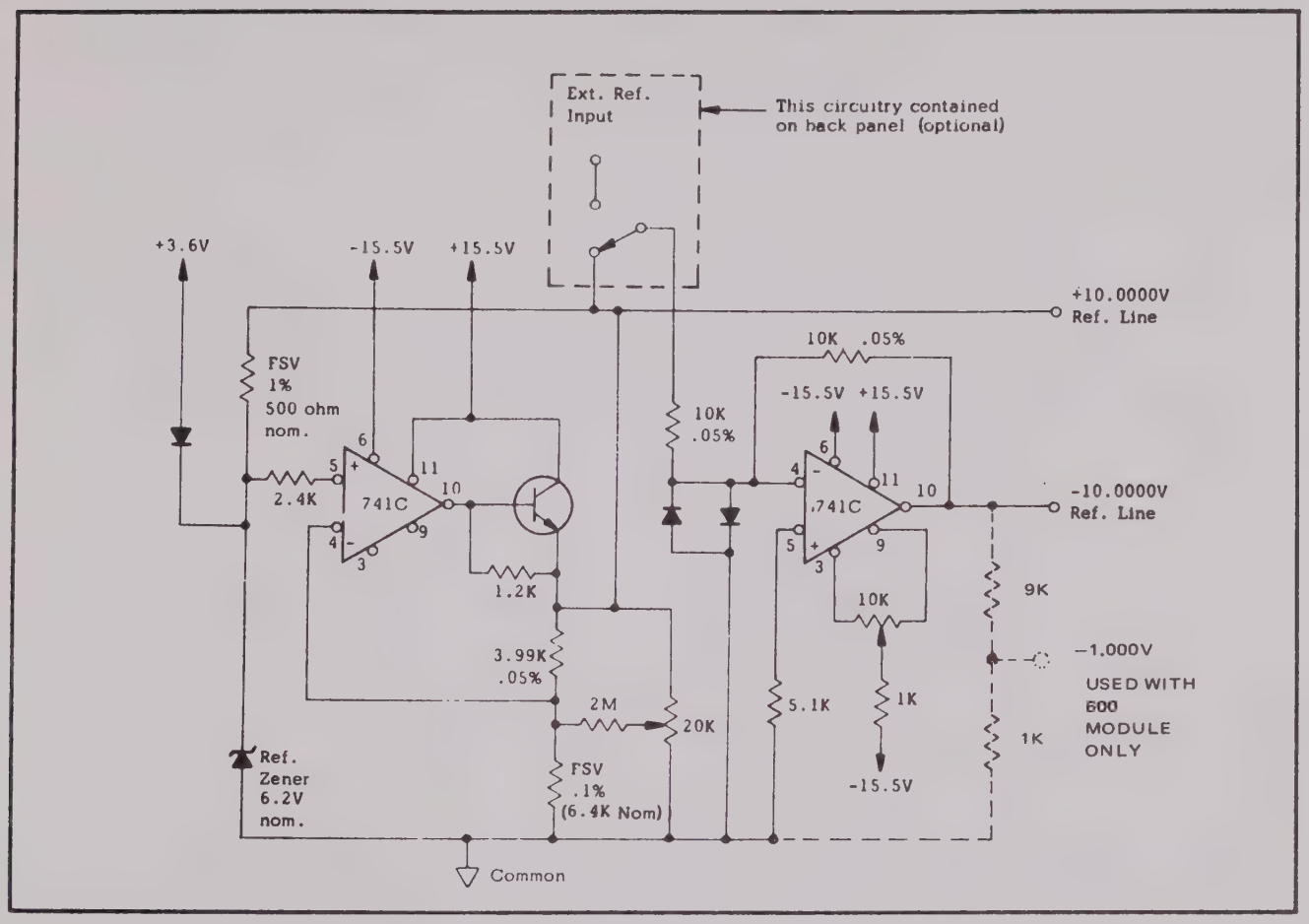


Figure 4.1 - Reference Supplies

the biasing current which will provide optimum temperature stability (TC). The selected resistor and zener are then installed in each DMM as a matched pair.

4.8 The +10V reference supply is designed around a differential amplifier connected as a non-inverting, potentiometric feedback amplifier. The feedback network sets the forward closed-loop gain of the amplifier at approximately 1.6. A potentiometer in the feedback circuit provides a "fine" adjustment of the gain for

calibration purposes. The reference zener and its biasing resistor are connected between the output of the +10V reference supply and circuit common. The cathode voltage of the reference zener provides the input signal to the amplifier in the +10V reference supply.

4.9 The -10V reference supply consists of a differential amplifier operated as an operational amplifier with a closed loop gain of one. Since an operational amplifier is an inverting amplifier, it simply inverts the +10V reference to -10V. The input impedance of an operational amplifier is equal to the value of the input summing resistor, which in this case is 10K. Therefore, the -10V supply draws only one milliampere from the +10V supply.

4.10 INTEGRATOR.

4.11 The integrator, shown in figure 4.2, is the center of the analog-to-digital conversion circuitry. It is designed around a high-gain differential amplifier. The circuit is connected as an operational amplifier, having a summing resistor of 200K ohms, and in the feedback element is a 0.55 microfarad capacitor. In operation, the circuit functions as outlined below.

4.12 Immediately prior to the beginning of a new reading the integrator is in a "reset" state. Its input and output are both at zero volts. When the instrument begins a new reading a solid-state switch Q21 closes, connecting the input of the Integrator to the output from the Signal Conditioning Module. At this point the out-

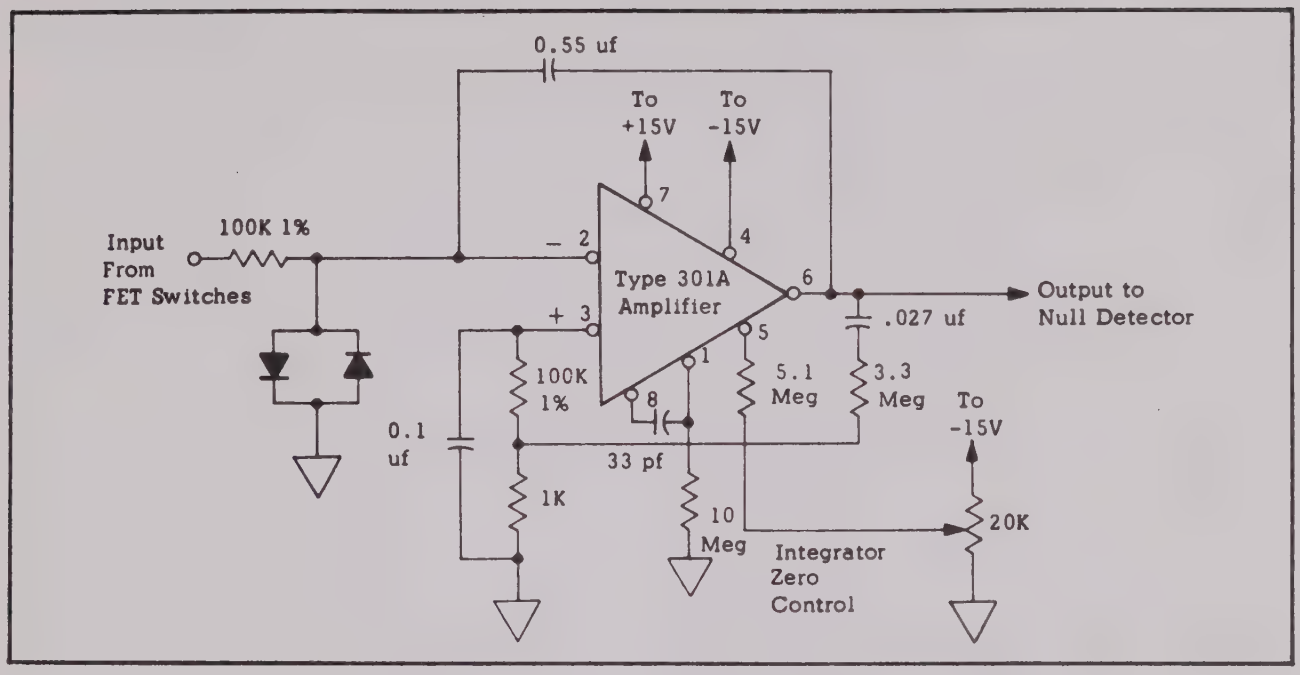


Figure 4.2 - Schematic, Integrator

put voltage from the integrator begins to move in a polarity opposite to the polarity of the voltage at its input. The Integrator's output voltage moves at a rate which is equal to the charging rate of the 0.55 microfarad feedback capacitor charged at a constant current which is equal to the $\frac{E}{R}$ relationship of the input voltage to the 200K ohm summing resistor. The amplifier acts as a constant current source which charges the capacitor. This charging of the feedback capacitor by a constant current source produces a linear ramp at the output of the Integrator, the change in whose voltage is given by the formula:

$$\Delta V = \frac{Ein\ Ts}{RC}$$

Where: ΔV = The change in voltage from the integrator

Ein = The input signal voltage

Ts = The fixed time that the switch connecting the Integrator's input to the input signal remains closed.

R = The Integrator's summing resistor

C = The value of the Integrators feedback capacitor.

4.13 The solid-state switch connecting the input of the Integrator to the signal voltage remains closed for a fixed period of time. This is referred to as the signal integration time (Ts). At the time that Ts begins, an oscillator of frequency f begins advancing the digital counter. The counter counts until a fixed number of counts (Cf) is reached.

4.14 When fixed count (Cf) is reached, the signal integration time (Ts) is terminated and the counter goes to zero. At this point the solid-state switch which connected the signal voltage to the Integrator's input opens and another switch closes connecting the Integrator's input to a precision 10V reference supply. This begins the reference integration period (Tr). The reference supply is opposite in polarity to the polarity of the input signal voltage. This causes the output voltage from the Integrator to ramp back toward zero until zero is reached, at which time the Null Detector senses the null state and causes the reference integrator time to be terminated. The counter accumulates oscillator counts from the beginning of Tr until Tr is terminated. At this time the counter contains a number of counts

(Cx), which is the number displayed in the DVM readout. Since Tr ends with the output voltage from the Integrator at the same level as when Ts started, the changes in voltage at the output of the Integrator must be equal and opposite:

$$\Delta V = \frac{-Eref\ Tr}{RC}$$

Where: ΔV = The change in output voltage from the Integrator

Eref = The voltage of the reference supply

Tr = The reference integration time

R = The value of the Integrator's summing resistor

C = The value of the Integrator's feedback capacitor

4.15 The measurement accuracy is entirely based upon the ratio of the signal integration time, a fixed number of counts (Cf), to the reference integration time, a variable number of counts (Cx). It is completely unaffected by oscillator frequency (f), or the RC components in the Integrator, provided only that these quantities remain stable during the time period required to take a measurement.

4.16 NULL DETECTOR.

4.17 The Null Detector, shown in figure 4.3, is a high gain non-inverting amplifier used to detect and signal the end of the reference integrate period. The Null Detector is designed around a high-gain differential amplifier. The circuit is of the potentiometric feedback type and has a closed-loop gain of 1100. The 20K resistor in series with the input and the two back-to-back diodes serve to

limit the input voltage to the null detector to ± 0.6 volts. The Null Detector has two outputs. One output goes directly to the digital circuits. The second output, a diode drop away from the first output, is applied to the FET Reset switch. The Reset switch is one of four FET switches connected to the input of the Integrator.

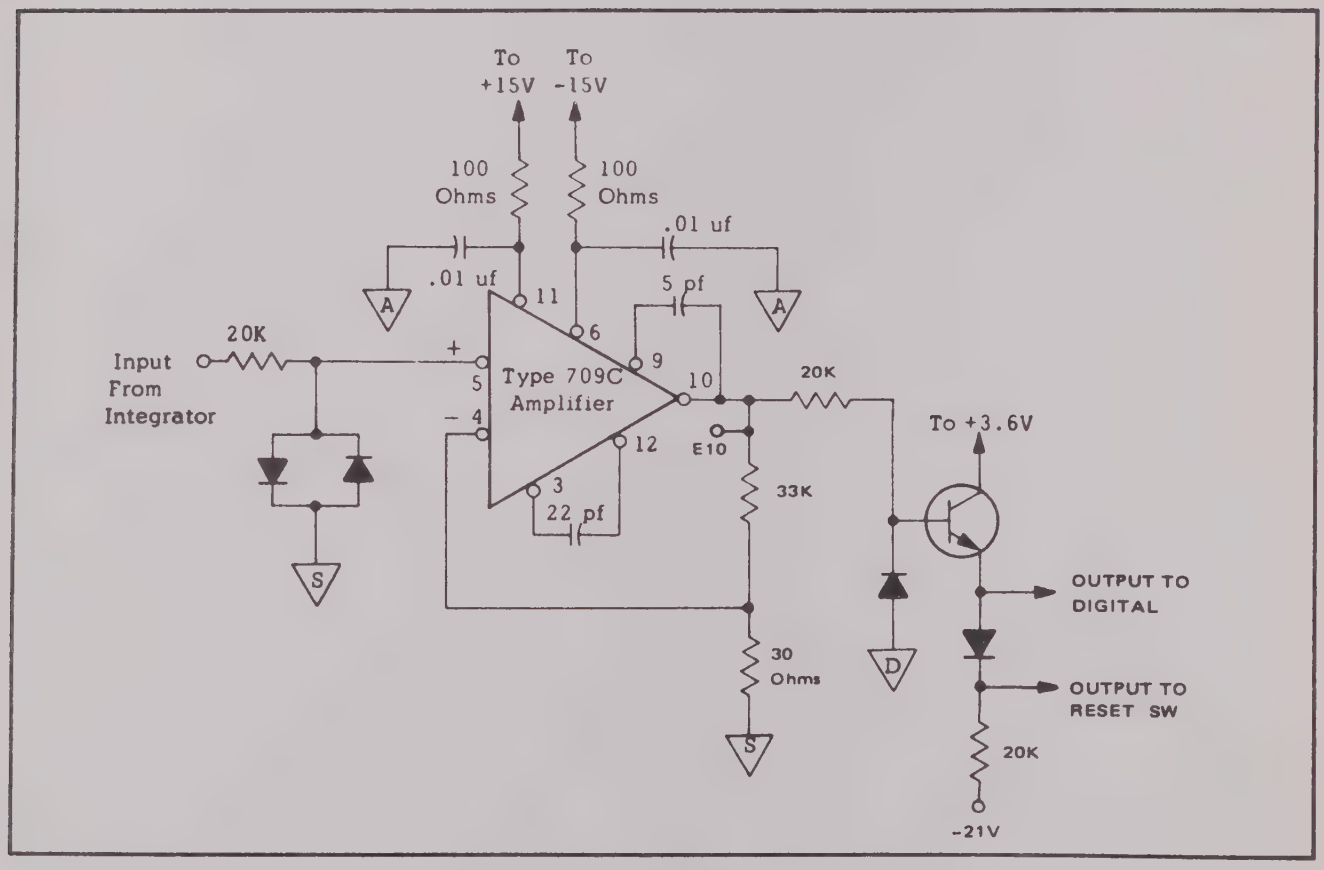


Figure 4.3 - Null Detector

4.18 OPERATION OF THE DIGITAL AND DISPLAY MODULE.

4.19 Figure 4.4 is a simplified version of the actual schematic which appears in the "drawings" section of this manual. As shown, all lines and logic levels

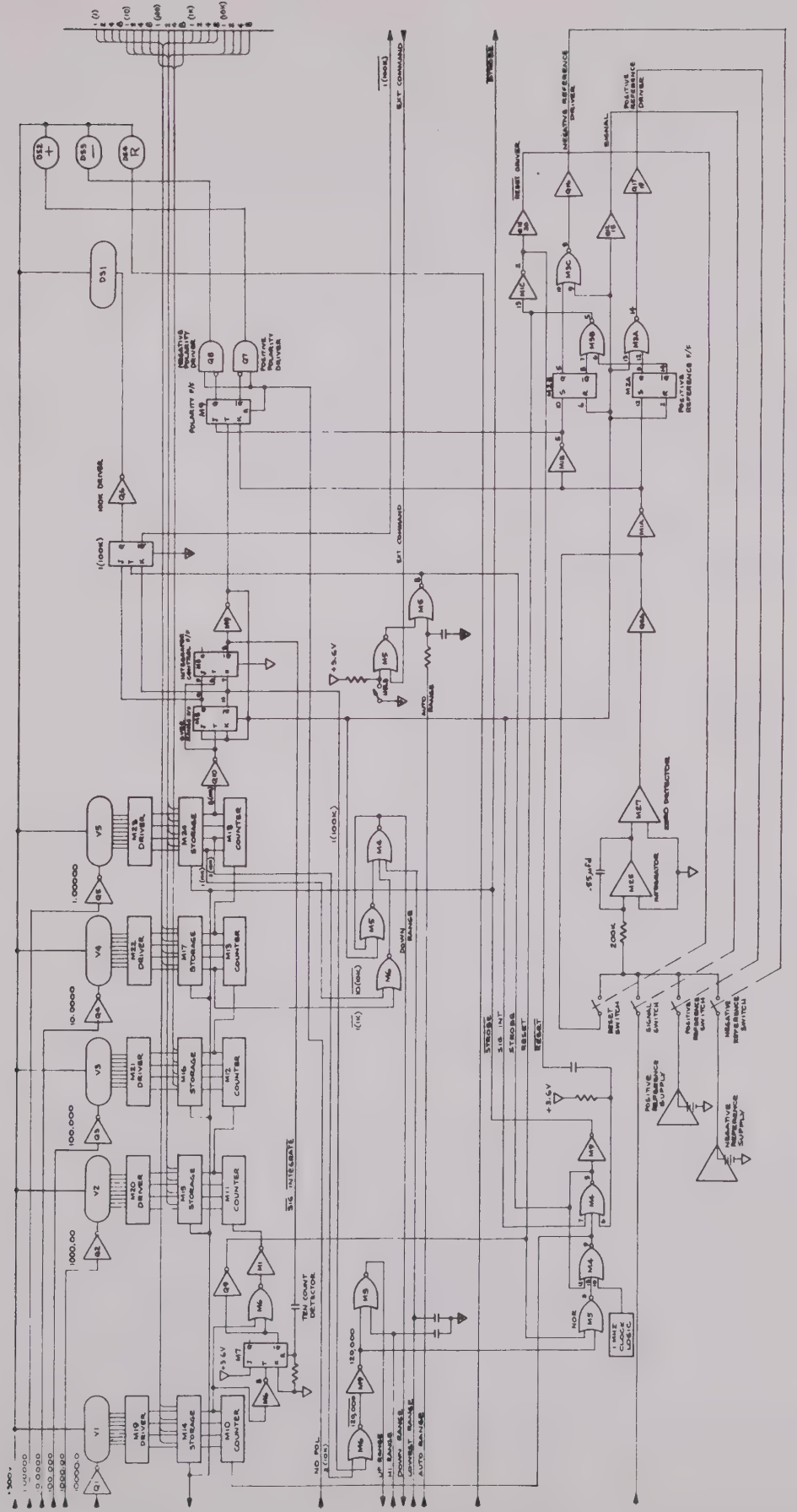


Figure 4.4 - Digitizing and Display Module - Simplified

are as they actually appear in the instrument. "Nor" gates which are used as inverters are shown as inverters and "nor" gates which are interconnected to form RS flip-flops are shown as RS flip-flops.

4.20 The counter consists of five individual decades and is continuously running and is never reset. The clock is gated to stop the counter whenever the instrument is in "hold" or during "strobe" time. A five decade counter can count only to 99999 whereupon it resets itself to 00000. A new reading is initiated every third time the counter reaches 00000.

4.21 At the beginning of each new reading the Signal Integrate line goes true. This closes the FET signal switch at the input to the integrator. The integrator begins to ramp up or down, depending on the polarity of the input signal. The signal integration ramp continues until the counter reaches 99999 and resets to 00000. At the moment the counter resets to 00000, the 80,000 line (which went true when the counter reached 80,000) goes false. This toggles the control flip-flop and the Signal Integrate line goes false. The Signal Integrate line going false disables the signal switch driver and the FET signal switch opens.

4.22 The polarity decision is made at the moment the counter resets from 099999 to 000000. If the input signal to the integrator is positive, the output voltage from the Integrator at the end of the signal integration time is negative. This causes the output voltage from the Null Detector to also be negative. This level is in-

verted by inverter M1A, setting the positive polarity line true (positive). The true level of the positive polarity line is inverted by inverter M1B, setting the negative polarity line false. If the polarity of the input signal were negative, the converse would be true.

4.23 Therefore, if the polarity of the input signal is positive, the positive polarity line is true and the negative polarity line false at the end of the signal integration period. If the polarity of the input signal is negative, the positive polarity line is false and the negative polarity line true at the end of the signal integration period.

4.24 When the signal integrate line goes false at the time the counter overflows to 000000, the polarity flip-flop toggles. The position taken by the polarity flip-flop is determined by the state of the positive polarity line and the negative polarity line at the end of the signal integration period. If the input signal is of positive polarity, the positive polarity line is true and the negative polarity line false. This causes the $\overline{Q}$ side of the polarity flip-flop to be set which enables driver Q7. Driver Q7 lights the + polarity light. If the input signal is of negative polarity the positive polarity line is false and the negative polarity line is true. This causes the Q side of the polarity flip-flop to be set which enables driver Q8. Driver Q8 lights the - polarity light.

4.25 During the signal integration period the signal integrate line is true. This holds the negative polarity flip-flop and the positive polarity flip-flop in a reset state. At the time the counter goes from 099999 to 000000 at the end of the signal

integration period, one or the other of these flip-flops toggles, depending on whether the positive polarity line or the negative polarity line is true. If the positive polarity line is true, the positive polarity flip-flop toggles, its Q output going true. This disables nor gate M3A, keeping the positive reference integrate line from going true when the signal integrate line goes false. Since the negative polarity flip-flop did not toggle, its Q output is false. This enables nor gate M3C as soon as the signal integrate line goes false. When nor gate M3C is enabled, the negative reference integrate line goes true, enabling the negative reference switch driver. The negative reference switch driver closes the FET negative reference switch.

4.26 At this point, the reference integration period begins and the output voltage from the integrator begins to ramp back toward zero volts. Had the input signal being measured been of negative polarity, the positive polarity line would have been false and the negative polarity line true at the end of the signal integration period. This would have caused the negative polarity flip-flop to toggle when the signal integrate line went false, leaving the positive polarity flip-flop in a reset state. This would have enabled nor gate M3A, setting the positive reference integrate line true (rather than the negative reference integrate line) and closed the negative reference switch.

4.27 At the moment the output voltage from the Integrator crosses zero (on the reference integration slope) the positive polarity line and negative polarity line change state. That is, whichever one was true goes false and whichever one was false goes true. This causes the remaining polarity flip-flop to toggle. Whichever one did not toggle at the beginning of the reference integration period

will do so at the end. This causes both nor gates M3C and M3A to be disabled so both the negative reference integrate line and the positive reference integrate line go (or remain) false. This opens both FET reference switches. When both the positive polarity flip-flop and the negative polarity flip-flop are in the set state, which occurs at the end of the reference integration period, nor gate M3B is enabled and the reset line goes true. This level is inverted by inverter M1C and the $\overline{\text{reset}}$ line goes false. This holds the output of the integrator at a level of zero volts.

4.28 When the reset line goes true at the end of the reference integration period, the strobe flip-flop is actuated through or gate M5. This causes the Q output of the strobe flip-flop to go true which actuates the strobe generator which is a 10 microsecond one-shot. The strobe generator causes the STROBE line to go true for a 10 microsecond period. This is inverted by inverter M9 and causes the $\overline{\text{STROBE}}$ line to go false for a 10 microsecond period. Then the STROBE line goes true, nor gate M4 is disabled, stopping the clock signals from reaching the counter for the duration of the strobe time. The negative level of the $\overline{\text{STROBE}}$ line gates the buffer storage units which translate whatever levels exist at their inputs at that moment to their outputs.

4.29 Information is stored at the outputs of the buffer storage units until the next negative transition of the $\overline{\text{STROBE}}$ line at the end of the next reading. The levels at the inputs of the buffer storage units are the output of the counter. Since the transition of the $\overline{\text{STROBE}}$ line which actuates the buffer storage units comes exactly at the end of the signal integration period, and at that time the state of the

counter represents the value of the voltage being measured, the reading displayed by the instrument equals the value of the signal voltage.

4.30 At the end of the 10 microsecond STROBE time, the strobe line again goes false and the $\overline{\text{STROBE}}$ line again goes true. When the strobe line goes false, nor gate M4 is again enabled and allows clock signals to reach the counter. The counter continues counting until it reaches 99999 whereupon it again resets itself to 00000. On this, the second transition of the counter from 99999 to 00000, the 80,000 line going false toggles the overrange flip-flop but does not again toggle the control flip-flop.

4.31 The overrange flip-flop did not toggle on the first transition of the 80,000 line, at the end of the signal integration period, because both its J and K inputs were held true by the signal integrate line which was true at that time. The control flip-flop does not re-toggle on the second transition of the 80,000 line because: a) the overrange flip-flop, at that time has not yet toggled at all so its Q output is still false and its $\overline{Q}$ output is still true; b) the J and K inputs of the control flip-flop are so connected that it cannot re-toggle until after the overrange flip-flop does.

4.32 The counter continues to count until it again reaches a count of 99999 and resets itself to 00000. At this point the 80,000 line again makes a transition from true to false. This time both the overrange flip-flop and the control flip-flop toggle. The overrange flip-flop is reset and the control flip-flop is set, causing the signal integrate line to go true, which initiates a new reading.

4.33 AUTO RANGE CIRCUITS.

4.34 In order to facilitate automatic ranging operation, uprange and downrange signals are generated by the Digitizing and Display Module. These signals command the range counter in the Signal Conditioning Module to count up or down. If the instrument is in too low a range for the signal voltage being measured the counter will reach a full-scale count of 120,000 prior to the zero-crossing of the output voltage of the integrator on the reference integration period. When this occurs, the 120,000 line goes true initiating strobe action. When this happens, the $\overline{120,000}$ line (which is normally always in a true state) goes false.

4.35 If the instrument is not already in the highest range, the highest range line into the Digitizing and Display Module will be false. This enables nor gate M3 setting the uprange line true. If the instrument is in too high a range for the signal being measured, null detection (and subsequently strobe) will occur before the counter reaches a count of 1000. This means that at the time strobe occurs the 1000 line is still false. If the instrument is not already in the lowest range the downrange flip-flop remains in a reset state. Its $\overline{Q}$ side is true setting the downrange line true. If the instrument is already in the lowest range the lowest range line is true. This causes the downrange flip-flop to be "set" as soon as the signal integrate line goes false at the end of the signal integrate period. When the downrange flip-flop is "set" its Q side is false causing the downrange line to be false. Whenever the count of the counter is between 1000 and 12,000 at the time the Integrator zero-crossing occurs the 1000 line is true so the downrange flip-flop is "set", resulting in no downrange signal and the 12,000 line is true, resulting in no uprange signal.

4.36 FET SWITCHING CIRCUITRY.

4.37 The four switches at the input to the Integrator are N-channel, field-effect, junction transistors. They are driven by circuitry composed of discrete components. The FET switches and their driving circuitry are shown in figure 4.5. The source and gate of each FET are connected to each other through fairly high value resistors (100K or 1 Meg). The gate of each FET connects to the driving circuitry through a series diode whose cathode connects to the collector of the driving transistor.

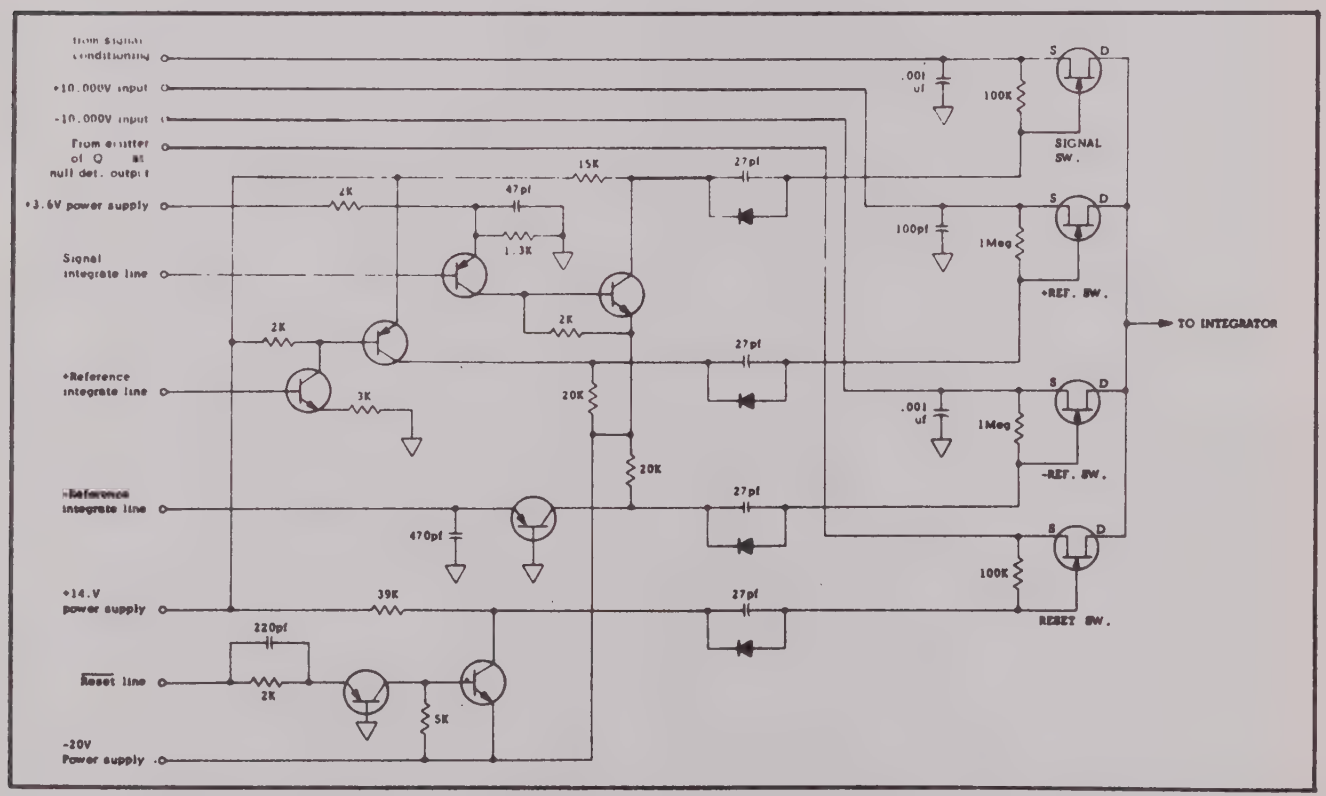


Figure 4.5 - Schematic, FET switches and switch drivers

4.38 In operation, the field-effect transistors are fully cut off (switch open) when the voltage at the gate, with respect to the source, is approximately -6V or more (-6V negative bias). When a FET is turned off, its driving transistor is either fully

saturated (as is the case with the signal integrate switch and the reset switch) or fully turned off (as is the case with the + Ref Switch and the - Ref Switch). In either case the net effect places its collector voltage at -20V. Since the cathode of the diode which connects to the gate of the FET is connected to the driver transistor's collector it too is at a -20V potential. Under this condition, the diode is forward biased. Current flows through the resistor which is connected between the source and gate of the FET. This produces a voltage drop across the resistor which places the FET's gate voltage at nearly -20V. Since no input signal to any of the FET switches is more negative than about -14V (under overload conditions) this assures that the FET is completely cut off.

4.39 When a FET is turned on (switch closed) its driver transistor's collector goes positive (relative to the most positive voltage that appears at the source of that particular FET). This causes the diode to be back biased so no current flows through it. Under this condition no current flows through the resistor connected between the source and gate of the FET so the source and gate are at the same potential (zero volts bias).

4.40 POWER SUPPLY.

4.41 The Power Supply Module provides all DC operating power to the instrument and it serves to interconnect the Digital and Display Module and the Signal Conditioning Module. It is constructed on a single printed circuit board. Both the Digital and Display Module and Signal Conditioning Module plug into sockets on the Power Supply Module.

4.42 The Power Supply, shown in figure 4.6, provides DC power to both the analog and digital portions of the instrument. Seven different voltage levels are provided. These are:

+28V	unregulated
-28V	unregulated
+15.5V	regulated
-15.5V	regulated
+3.6	regulated
+300V	unregulated
+150V	unregulated

4.43 The power transformer has three secondary windings which step the AC line voltage to three different levels. The 300V winding provides power for the +300V and +150V supplies. The 6V winding supplies power for the +3.6V supply and the 56V winding provides power for the positive and negative 28V and 15.5V supplies.

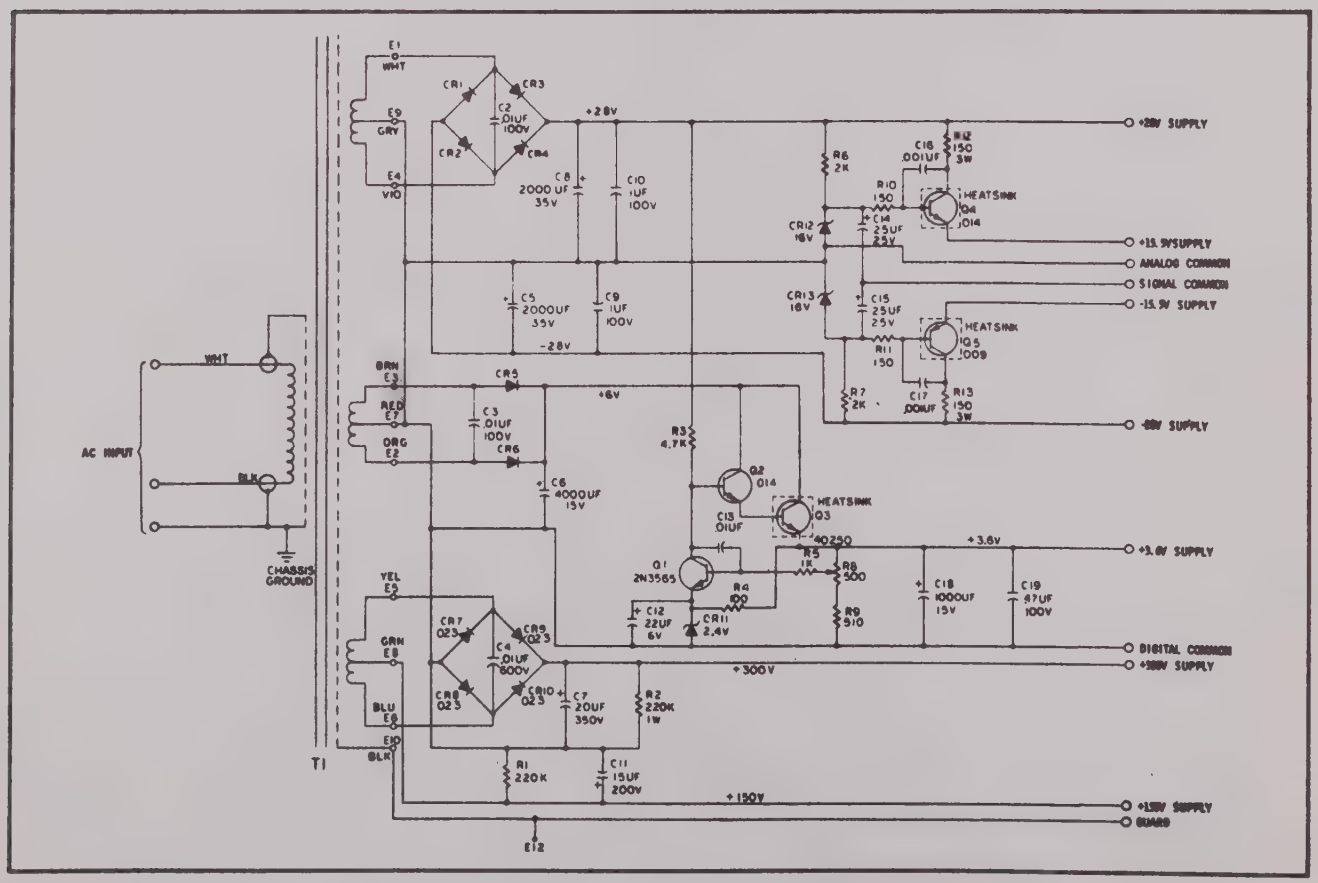


Figure 4.6 - Power Supply

4.44 Diodes CR-7 through 10 form a full wave bridge type rectifier whose input is connected across the 300V winding of the power transformer. The output of the bridge rectifier is connected across capacitor C7 which is the filter capacitor for the +300V line. Resistor R2 is connected across capacitor C7 as a bleeder resistor to eliminate shock hazard. The +150V DC output is taken from the center tap of the 300V transformer winding. Capacitor C11 is the filter capacitor for the +150V DC line. Resistor R1 is the bleeder resistor for capacitor C11.

4.45 Diodes CR-1 through 4 are shown on the schematic diagram connected across the 56V transformer winding as a bridge. In operation, however, they do not function in exactly the same manner as a conventional full wave bridge rectifier. The winding is center tapped and this point is connected to digital common (ground). Diodes CR-3 and CR-4 form a full wave rectifier which charge capacitor C8 to +28V DC. C8 is connected between the +28V line and digital common and is the +28V filter capacitor. Similarly, diodes CR-1 and CR-2 form a full wave rectifier which charges capacitor C5 to -28V DC. C8 is connected between the -28V line and digital common and is the filter capacitor.

4.46 Transistors Q4 and Q5 are series regulators which reduce the +28V to +15.5V and -28V to -15.5V respectively. Zener diodes CR-12 and CR-13 clamp the bases of these transistors at a 16V level. The voltages at the emitters of these transistors are always about 0.6V less than that at the bases and since the voltage at the bases is clamped by the zeners the 15.5V lines are regulated. Resistors R12 and R13, in series with the collectors of the regulator transistors, provide protection

for the transistors in the event of an accidental short circuit between either 15.5V supply line and circuit common. The digital, analog, and signal commons all connect together in the Signal Conditioning Module. Capacitors C14 and C15 filter zener noise and keep it off the 15.5V lines.

4.47 The 6V winding of the power transformer is connected to circuit common. Diodes CR-5 and CR-6 and the center tap of the winding form a full wave rectifier which charges filter capacitor C6. In operation the voltage across capacitor C6 is approximately +6V DC with respect to circuit common. Transistor Q3 is a series regulator transistor which converts the +6V to +3.6V. Transistors Q2 and Q3 are connected in a Darlington configuration. The current gain of Q3 is thus multiplied by the current gain of Q2. Base drive for the Darlington connected regulator transistors is provided by resistor R3 which connects to the +28V line. It is controlled by the collector current through transistor Q1.

4.48 Base bias for transistor Q1 comes through resistor R5 which connects to the wiper of potentiometer R8. Zener diode CR-11 clamps the voltage at the emitter of transistor Q1 at +2.4V. This forces the voltage at Q1's base to always be approximately +3V. This causes any voltage change at the wiper of potentiometer R8 to result in a directly proportional change in the current through resistor R5. Since this is the current controlling transistor Q2, the zener acts as a reference element which stabilizes the output voltage of the supply.

4.49 Potentiometer R8 is adjusted to set the collector current through transistor Q1. The potentiometer is adjusted to a point to give enough base drive to the Darlington circuit to keep the emitter voltage of transistor Q3 at exactly +3.6V.

If the voltage at the emitter of Q3 should drop (due to a change in either the line voltage or level current) the available base drive to transistor Q1 will also decrease. This will cause less collector current to flow through transistor Q1. More current is available as base drive for the regulator transistors. This current turns transistor Q3 on harder and raises the emitter voltage back to +3.6V.

SECTION 5

CALIBRATION

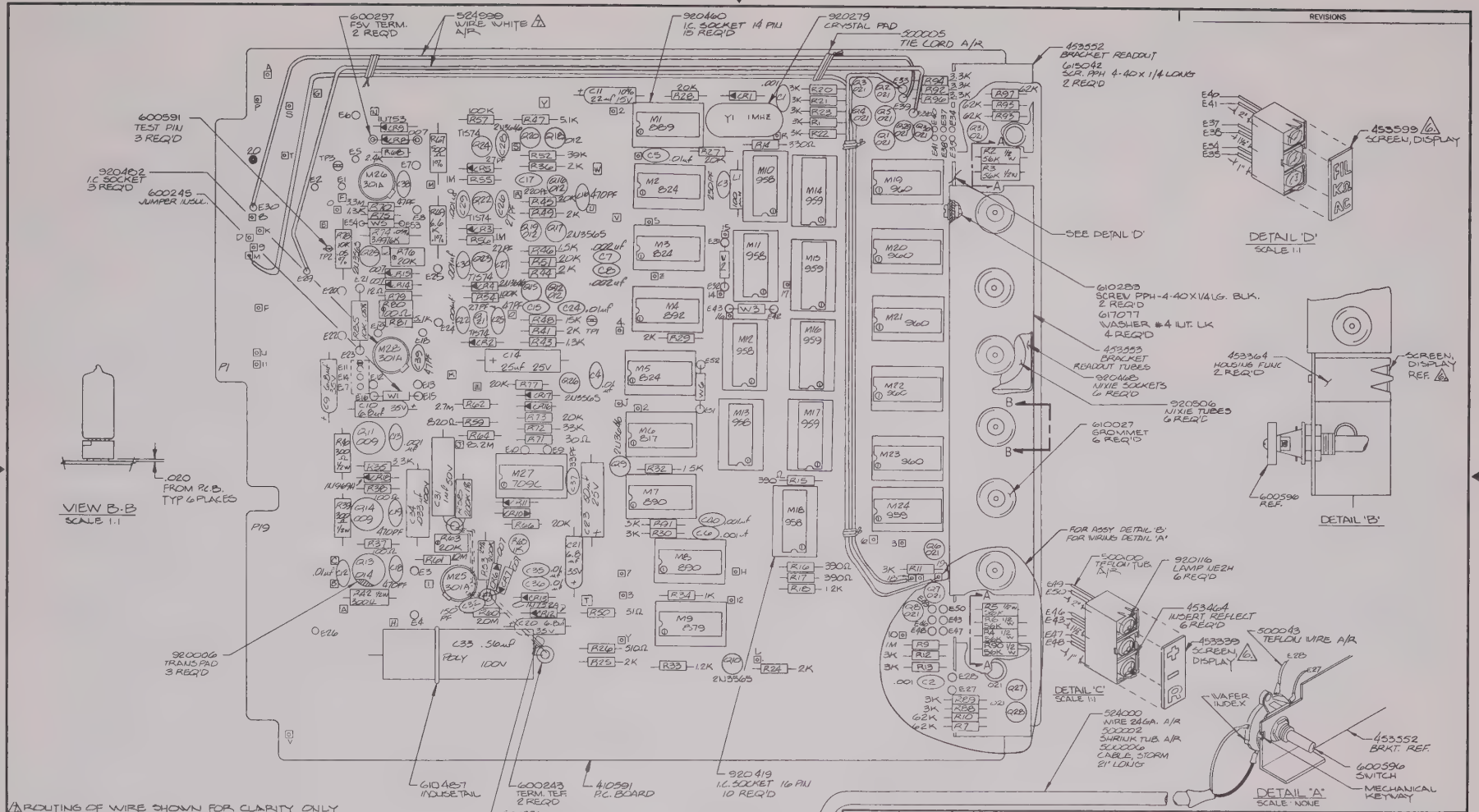
5.1 Since calibration procedures are dependent on the model of Signal Conditioning Module used, please refer to the appropriate Signal Conditioning manual, Section 5, for calibration procedures.

SECTION 6

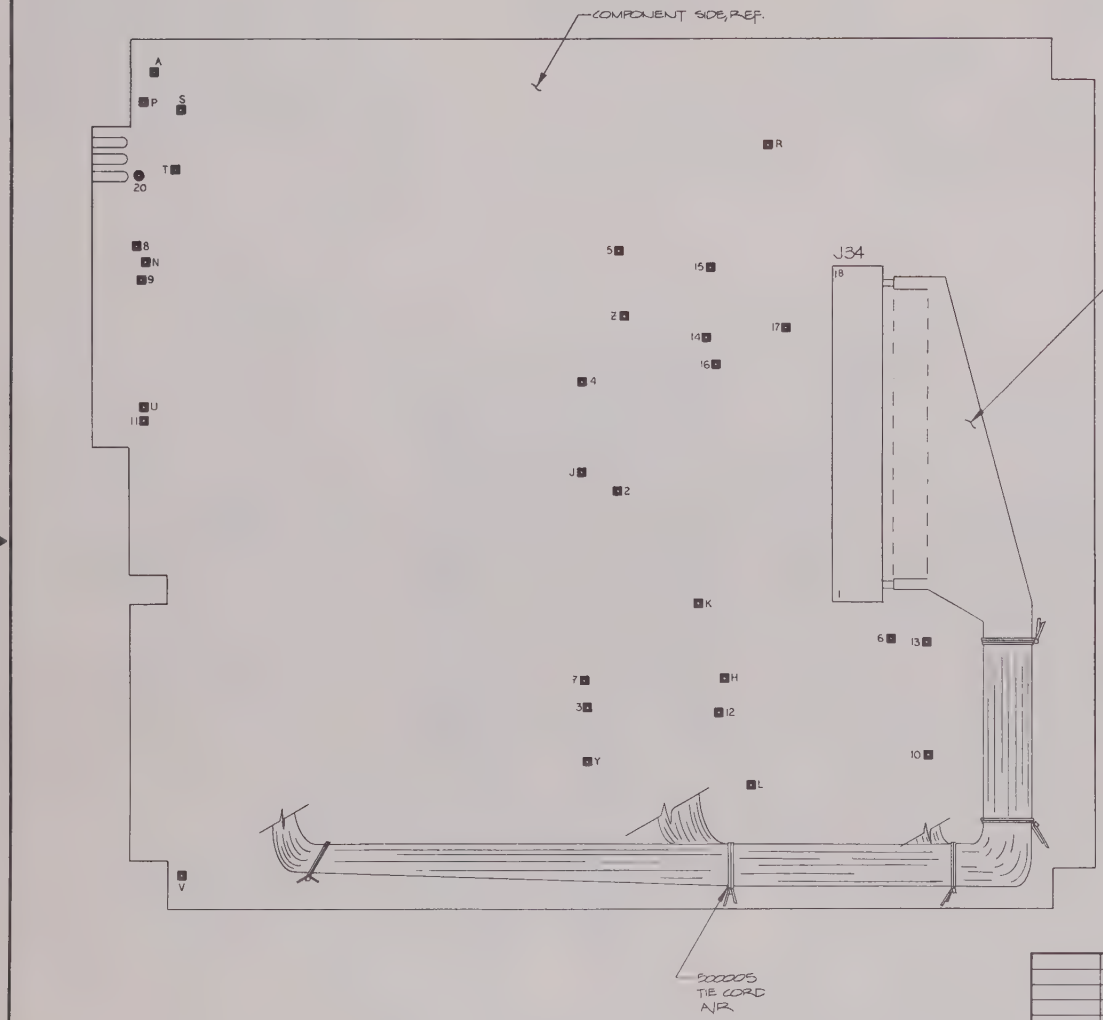
DRAWINGS

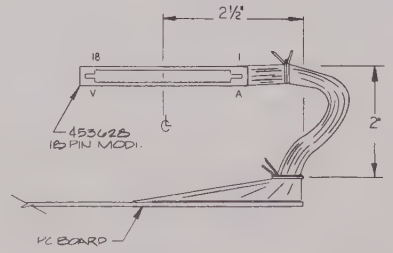
6.1 DRAWINGS.

PCB Assembly, Readout	403484
Schematic, Readout	430974
Assembly, Power Supply	403508
PCB Assembly, Power Supply	403081
Schematic, Power Supply	430842
Assembly, Rear Panel	403509
Ratio Option 5330	403453
PCB Assembly, Reference Buffer	403452
Schematic, Ratio Option	430962
Model 95 BCD Output Option	403505
PCB Assembly, Model 95	403487
Schematic, Model 95	430979
Analog Output	403262
Rear Input, 4-wire	403512
Assembly, Isolated Power Supply	403495
Schematic, Isolated Power Supply	430978
Schematic, Interconnection	430983


REVISIONS
600297 FSV TERM. 2 REQ'D
524000 WIRE WHITE A/R
920460 I.C. SOCKET 14 PIN 15 REQ'D
920279 CRYSTAL PAD
500005 TIE CORD A/R
453552 BRACKET READOUT
615042 SCR. PPH 4-40 X 1/4 LONG 2 REQ'D
600591 TEST PIN 3 REQ'D
920462 I.C. SOCKET 3 REQ'D
600245 JUMPER WIRE
453599 SCREEN, DISPLAY
DETAIL 'D'
SCALE 1:1
SEE DETAIL 'D'
610289 SCREW PPH-4-40X1/4LG. BLK. 2 REQ'D
617077 WASHER #4 INT. LK 4 REQ'D
453553 BRACKET READOUT TUBES
920468 NIXIE SOCKETS 6 REQ'D
920506 NIXIE TUBES 6 REQ'D
610027 GROMMET 6 REQ'D
453464 HOUSING FUNC 2 REQ'D
SCREEN, DISPLAY REF.
600596 REF.
DETAIL 'B'
VIEW B-B
SCALE 1:1
.020 FROM P.C.B. TYP 6 PLACES
FOR ASSY DETAIL 'B' FOR WIRING DETAIL 'A'
500006 TEFLON TUB. A/R
920116 LAMP UE2H 6 REQ'D
453464 INSERT REFLECT 6 REQ'D
453339 SCREEN DISPLAY
500043 TEFLON WIRE A/R
DETAIL 'C'
SCALE 1:1
WAFER INDEX
524002 WIRE 24GA. A/R
500002 SHRINK TUB. A/R
500006 CABLE STORM 21" LONG
453552 BRKT. REF.
600596 SWITCH
MECHANICAL KEYWAY
DETAIL 'A'
SCALE - NONE
920006 TRANS PAD 3 REQ'D
610457 INDUCTAIL
600243 TERM. TEF. 2 REQ'D
410591 P.C. BOARD
920419 I.C. SOCKET 16 PIN 10 REQ'D
501376 TEFLON TUBING A/R
600378 PLUG 600380 PIN 3 REQ'D
VIEW A-A
2 PLACES
1/16"
ROUTING OF WIRE SHOWN FOR CLARITY ONLY ROUTE ALL WIRES DIRECTLY TO EACH POINT.
BOND 453559 TO BRKT. 453553 W/920008 EASTMAN 910.
FOR RATIO OPTION INFORMATION SEE
ALL DIODES 018.
ALL RESISTORS ARE IN OHMS ±5%, 1/4 W. CARBON.
SCHEMATIC REF. 430974
ASSY PROCEDURES & PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS.
NOTES: UNLESS OTHERWISE SPECIFIED
5333
NEXT DWG
USED ON
APPLICATION
QTY REQD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES
DECIMALS X .020 XX .020 XXX .010
ANGLES 0° 30' FORMED 1° 0'
HOLE DIAMETERS ±.004 -.001
DIMENSIONS AND TOLERANCES PER USAS Y14.15
MATERIAL
FINISH
DRAWN K.R. CUNNINGHAM 10-5-70
CHECK 3/2/71
DESIGN 3/4/71
MECH ENGR
PROJ ENGR 3/5/71
PROG ENGR 3/6/71
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
ASSY READOUT
SIZE D
CODE IDENT NO. 21793
DWG NO. 403484
REV A
SCALE 2:1
SHEET 1 OF 10

REVISIONS





DETAIL "A"
SCALE 1:1

POINT ON READOUT BD	CONN. J34	COLOR	AWG #24 VINYL INSUL.
2	9	RED	524222
A	A&1	BLACK	524000
V	V&18	BLACK	524000
U	5	W BR BR	524911
10	3	W BR R	524912
9	C	W BR OR	524913
B	4	W BR YL	524914
T	M	W BR GR	524915
S	N	W BR BLU	524916
R	14	W BR V	524917
N	L	W BR G	524918
P	K	W BR W	524919
5	P	W R BK	524920
11	D	W R BR	524921
3	J	W R R	524922
4	B	W R OR	524923
H	12	W R YL	524924
Y	R	W R GR	524925
Z	13	W R BLU	524926
L	15	W R V	524927
20	2	W R G	524928
13	7	W R	524929
12	H	W OR BK	524930
6	E	W OR BR	524931
7	6	W OR R	524932
15	T	GRN.	524555
14	5	W OR YL	524934
16	16	W OR GR	524935
17	17	W OR BLU	524936
K	U	WHITE	524999

SEE SHEET 1.
NOTES. UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT ASSY	FINAL ASSY
403511	5333		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0 30'	+.004
XX .020	FORMED	-.001
XXX .010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

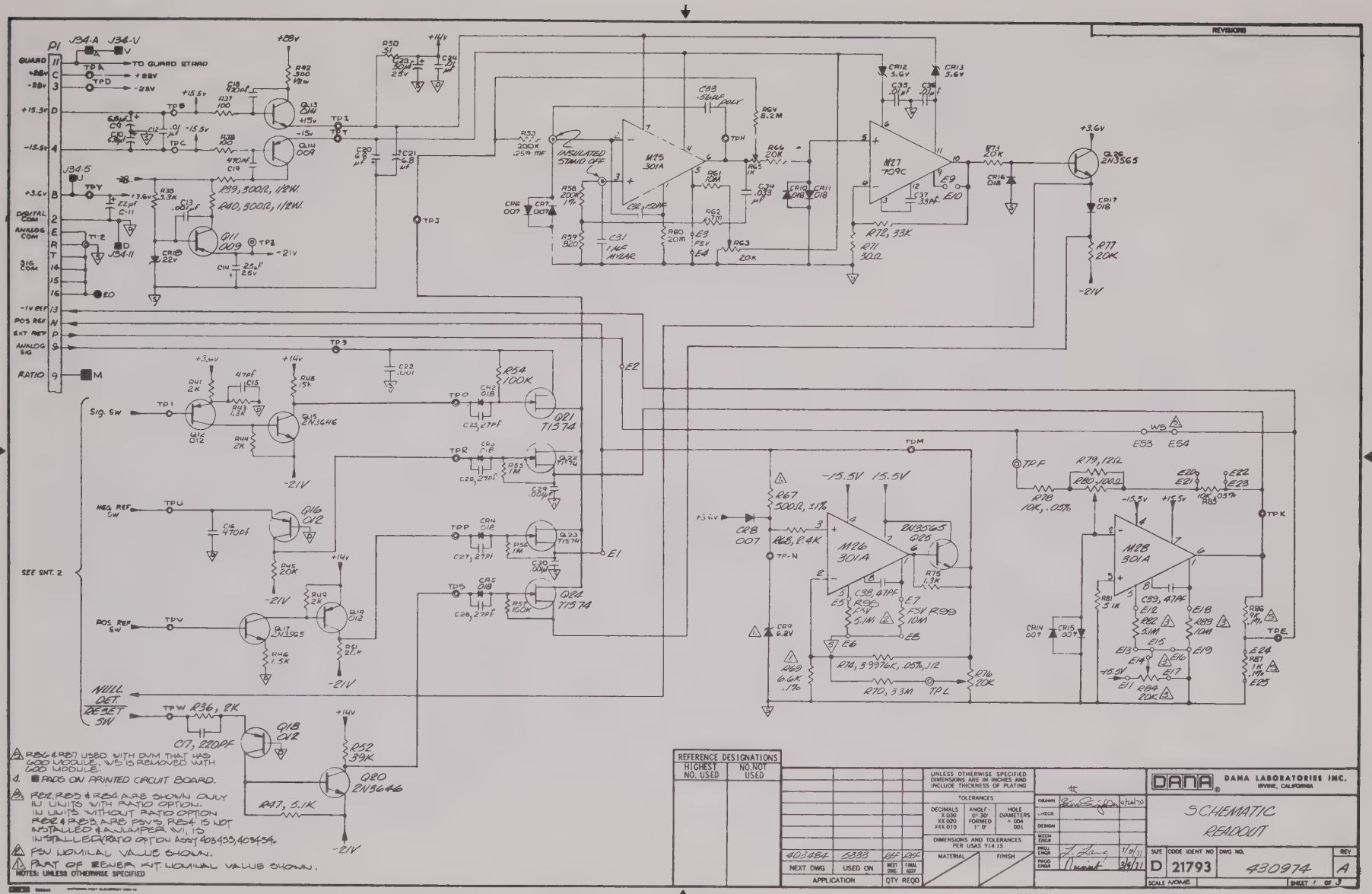
DRAWN	K. M. Cunningham	Jan. 4, 1971
CHECK	[illegible]	2/2/71
DESIGN	[illegible]	2/2/71
MECH ENGR		
PROJ ENGR	[illegible]	2/5/71
PROD ENGR	[illegible]	3/8/71

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY P.C. BOARD READOUT

SIZE	CODE IDENT NO.	DWG NO	REV
D	21793	403484	A

SCALE 2:1 SHEET 2 OF 10



REVISIONS

REFERENCE DESIGNATIONS	
HIGHEST NO. USED	NO. NOT USED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

403484	5333		
NEXT DWG	USED ON	NOT DWG.	FINAL ASST
APPLICATION		QTY REQD	

MATERIAL | FINISH

DRAWN		4/28/70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		3/9/71
PROD ENGR		3/6/71

DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC READOUT

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	430974	A

SCALE NONE | SHEET 1 OF 3

△A R86 & R87 USED WITH DVM THAT HAS GOOD MODULE. W5 IS REMOVED WITH GOOD MODULE.

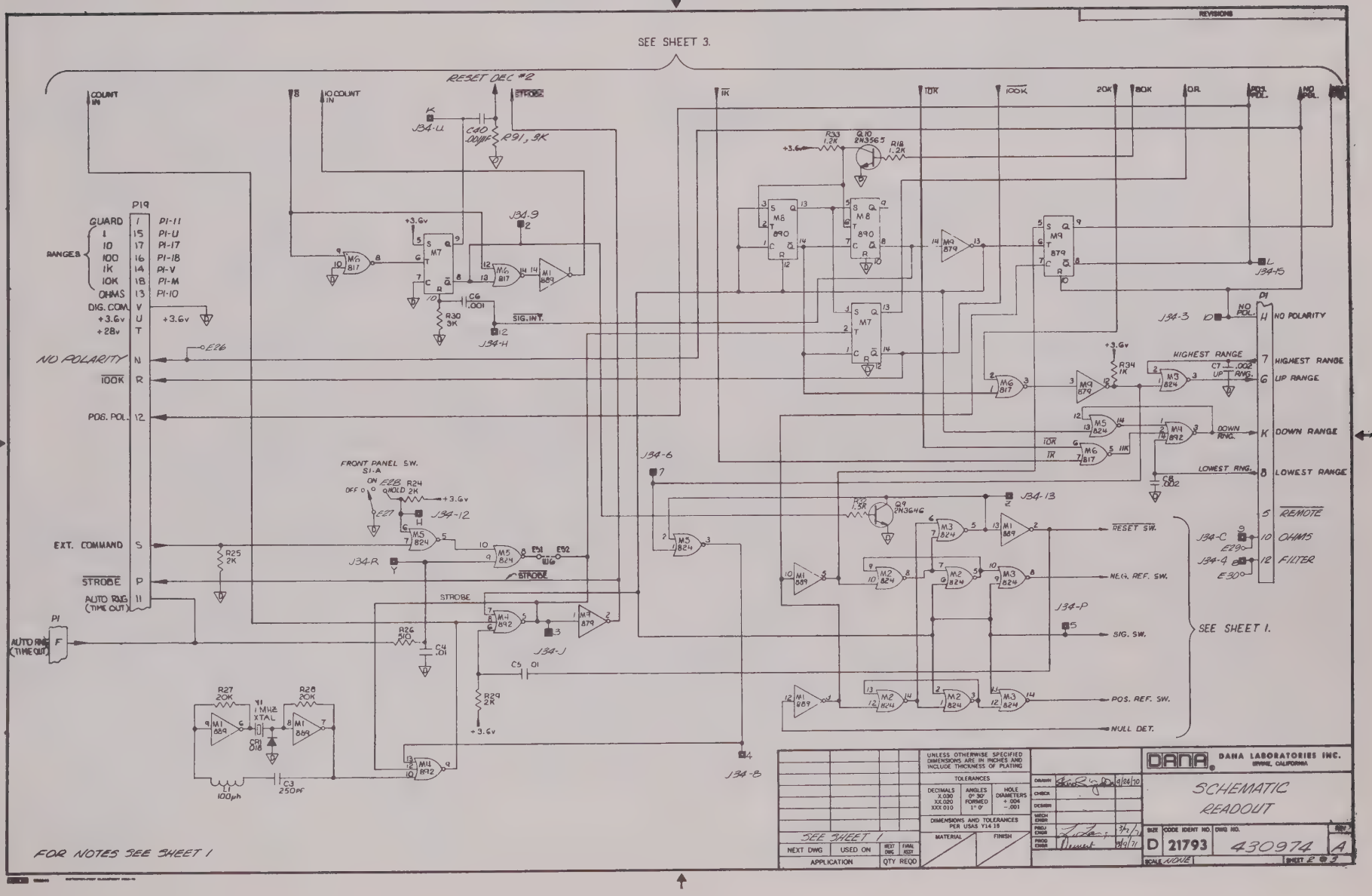
1. ■ PADS ON PRINTED CIRCUIT BOARD.

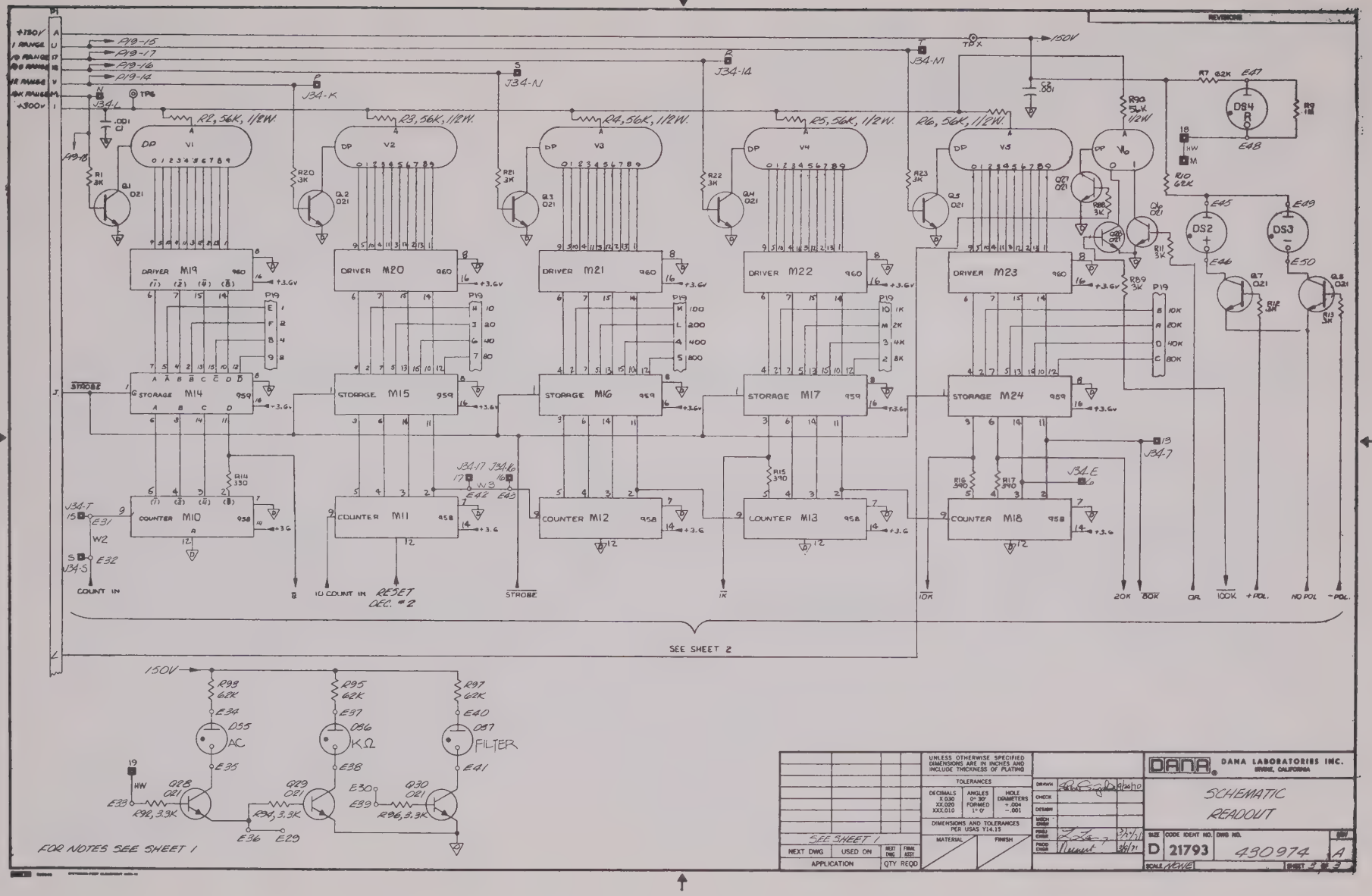
△B R82, R83 & R84 ARE SHOWN ONLY IN UNITS WITH RATIO OPTION. IN UNITS WITHOUT RATIO OPTION R82 & R83 ARE FSV'S R84 IS NOT INSTALLED & A JUMPER W1, IS INSTALLED(RATIO OPTION ASSY 403453, 403454).

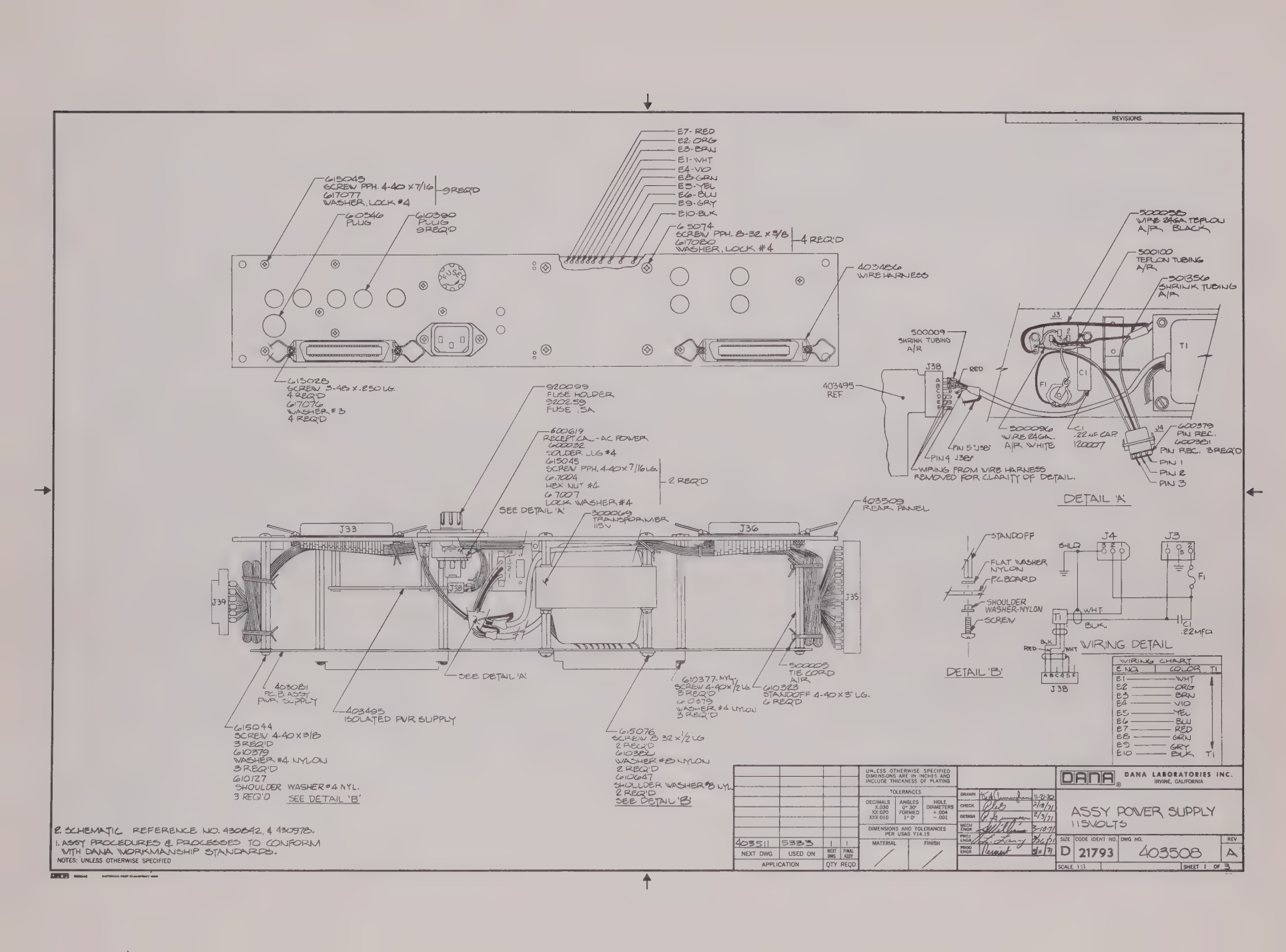
△C FSV NOMINAL VALUE SHOWN.

△T PART OF GENERA KIT. NOMINAL VALUE SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED


SEE SHEET 3.
REVISIONS
RESET DEC #2
COUNT IN
10 COUNT IN
STROBE
1K
10K
100K
20K
80K
O.R.
POS. POL.
NO POL.
P19
GUARD
RANGES
DIG. COM.
+3.6v
+28v
OHMS
NO POLARITY
100K
POS. POL.
EXT. COMMAND
STROBE
AUTO RNG (TIME OUT)
P1
R91, 3K
C60 .0047MF
R30 3K
C6 .001
SIG. IN.
R33 1.2K
R18 1.2K
Q10 2N3565
R34 1K
C7 .002 UP RNG.
C8 .002
HIGHEST RANGE
UP RANGE
DOWN RNG.
DOWN RANGE
LOWEST RNG.
LOWEST RANGE
REMOTE
OHMS
FILTER
FRONT PANEL SW. S1-A
R24 2K
R25 2K
R26 510
C4 .01
C5 .01
R29 2K
R30 1.5K
Q9 2N3646
RESET SW.
NEG. REF. SW.
SIG. SW.
POS. REF. SW.
NULL DET.
SEE SHEET 1.
R27 20K
R28 20K
Y1 1 MHz XTAL
CR1 D18
L1 100μh
C3 250PF
J34-4
J34-6
J34-8
J34-9
J34-12
J34-13
J34-15
J34-R
J34-P
E26
E27
E28
E29
E30
E31
E32
SEE SHEET 1
FOR NOTES SEE SHEET 1
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES
DECIMALS X.030 XX.020 XXX.010
ANGLES 0° 30' FORMED 1° 0'
HOLE DIAMETERS +.004 -.001
DIMENSIONS AND TOLERANCES PER USAS Y14.1B
MATERIAL
FINISH
NEXT DWG
USED ON
APPLICATION
NEXT ASSY
FINAL ASSY
QTY REQD
DRAWN
CHECK
DESIGN
WATCH ENGR
PROJ ENGR
PROD ENGR
8/26/70
3/1/71
8/9/71
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC
READOUT
SIZE D
CODE IDENT NO. 21793
DWG NO. 430974
REV A
SCALE NONE
SHEET 2 OF 3


REVISIONS
+150V
I RANGE
10 RANGE
100 RANGE
1K RANGE
10K RANGE
+300V
J34-L
J34-K
J34-N
J34-14
J34-M
150V
TP6
TP7
R1, 56K, 1/2W.
R2, 56K, 1/2W.
R3, 56K, 1/2W.
R4, 56K, 1/2W.
R5, 56K, 1/2W.
R6, 56K, 1/2W.
R7 62K
R8 1M
R9 51K 1/2W
R10 62K
R11 3K
R88 3K
R89 3K
R90 3K
R91 3K
R92 3K
R93 3K
R94 3K
R95 3K
R96 3K
R97 3K
R114 330
R115 390
R116 390
R117 390
DRIVER M19
DRIVER M20
DRIVER M21
DRIVER M22
DRIVER M23
STORAGE M14
STORAGE M15
STORAGE M16
STORAGE M17
STORAGE M24
COUNTER M10
COUNTER M11
COUNTER M12
COUNTER M13
COUNTER M18
STROBE
COUNT IN
10 COUNT IN
RESET DEC. #2
SEE SHEET 2
DS4
DS2
DS3
DS5 AC
DS6 KΩ
DS7 FILTER
FOR NOTES SEE SHEET 1
SEE SHEET 1
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC
READOUT
SIZE D
CODE IDENT NO. 21793
DWG NO. 430974
REV A
SCALE NONE
SHEET 3 OF 3



2. SCHEMATIC REFERENCE NO. 430842, & 430578.
1. ASSY PROCEDURES & PROCESSES TO CONFORM WITH DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

403511	5333	1	1	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX 020	FORMED	-.001
XXX 010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

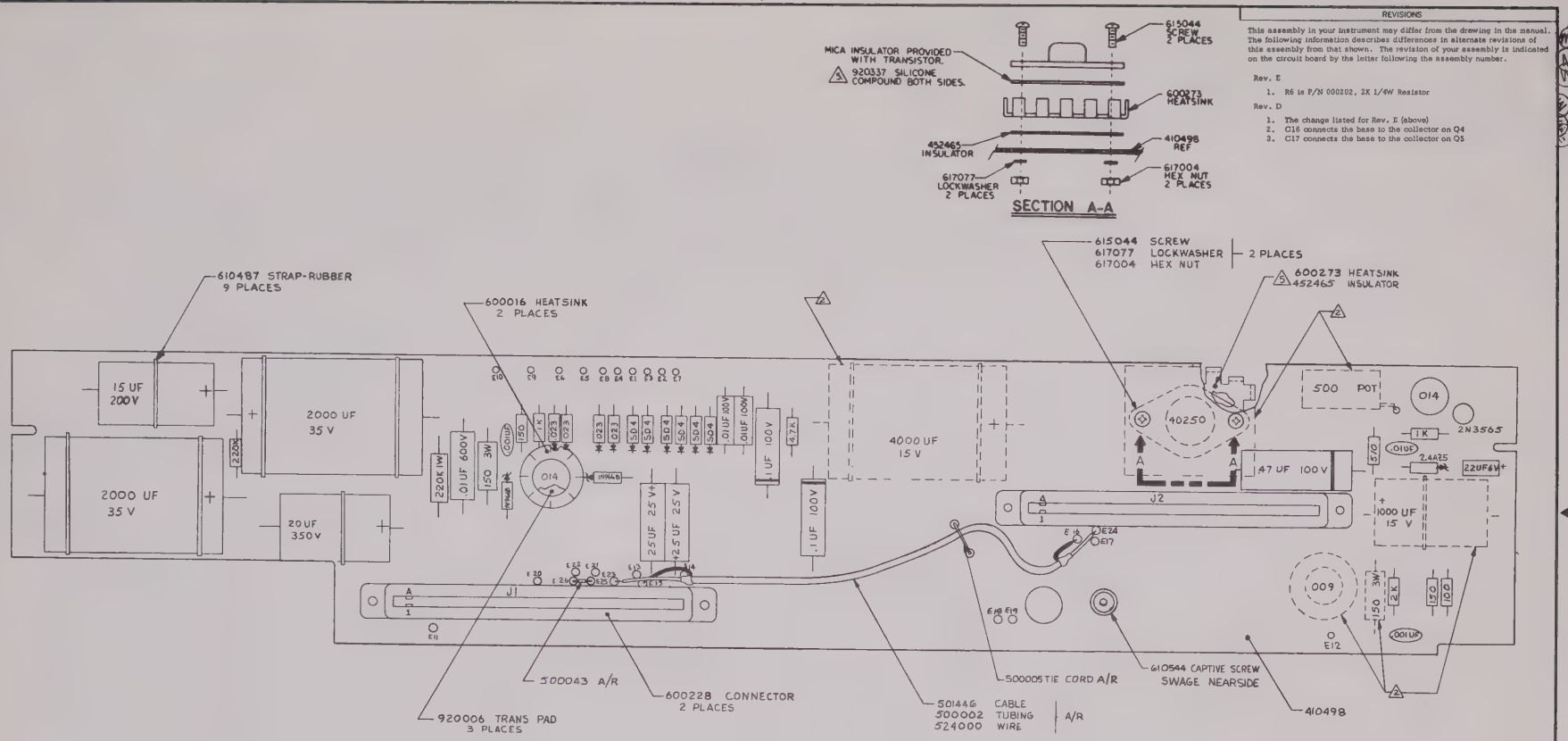
MATERIAL / FINISH

DRAWN		11-21-70
CHECK		2/18/71
DESIGN		2/3/71
MECH ENGR		3-10-71
PROJ ENGR		3/26/71
PROD ENGR		3/31/71

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

ASSY POWER SUPPLY 115VOLTS

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403508	A
SCALE 1:1			SHEET 1 OF 3



REVISIONS

This assembly in your instrument may differ from the drawing in the manual. The following information describes differences in alternate revisions of this assembly from that shown. The revision of your assembly is indicated on the circuit board by the letter following the assembly number.

Rev. E

1. R6 is P/N 000202, 2K 1/4W Resistor

Rev. D

1. The change listed for Rev. E (above)
2. C16 connects the base to the collector on Q4
3. C17 connects the base to the collector on Q5

5. PUT SILICONE COMPOUND 920337 ON BOTH SIDES OF THE MICA INSULATOR PROVIDED WITH THE 40250 PWR TRANSISTOR.
4. ALL RESISTORS ARE IN OHMS 1/4W, ± 5% CARBON
3. REF SCHEMATIC NO. 430842.
2. COMPONENTS LOCATED FARSIDE.
1. ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403203	4630	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30' FORMED 1° 0'	+ .004 - .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

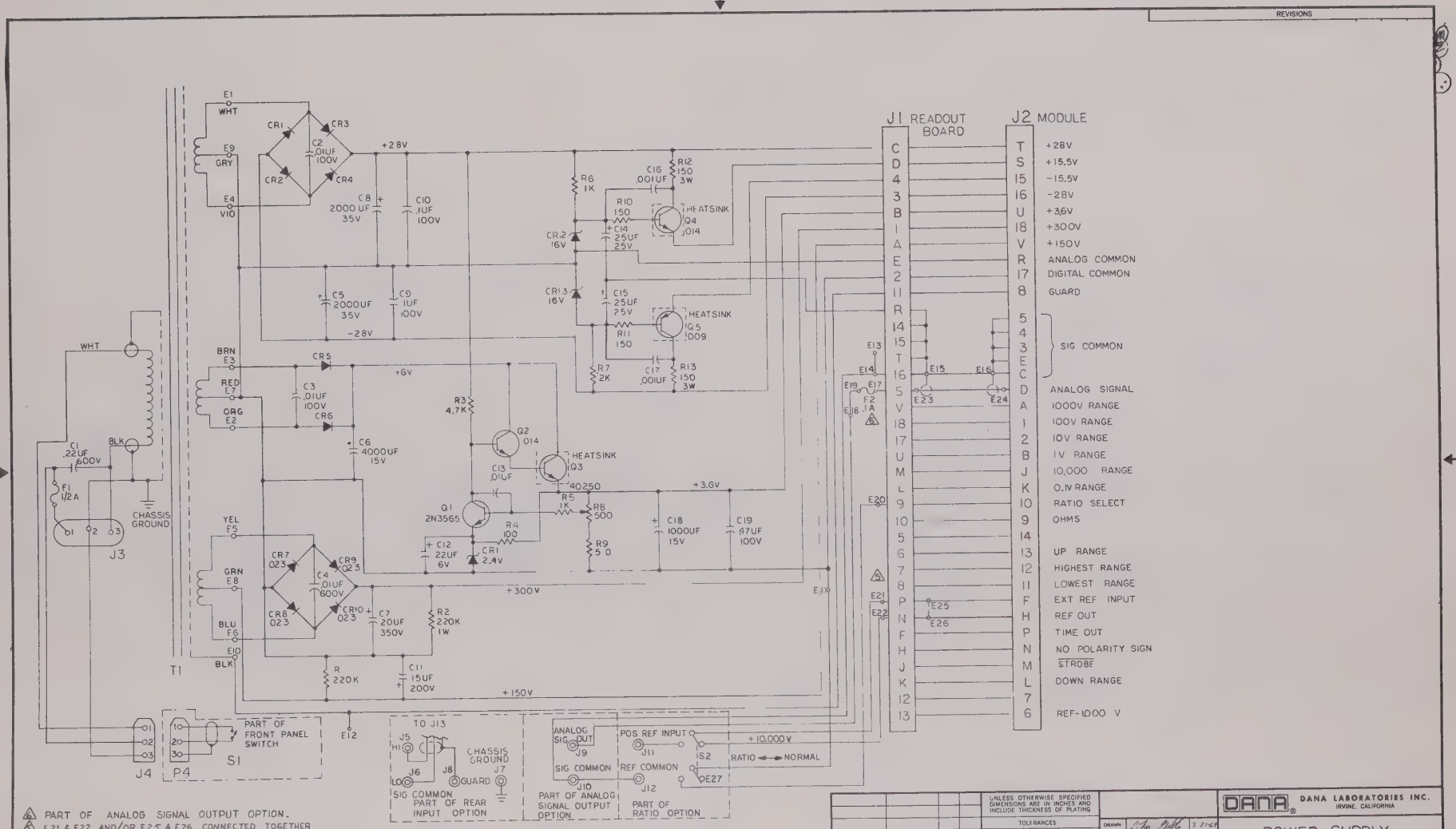
DRAWN	CT Wellmon	4-9-69
CHECK	W Graben	4-30-69
DESIGN	J Summers	5/16/69
MECH ENGR		
PROJ ENGR	L Ford	5/16/69
PROD ENGR	D Stubbs	5/16

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PC BOARD ASSY POWER SUPPLY FULL RACK

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403081	F

SCALE 2/1 SHEET 1 OF 3



4. PART OF ANALOG SIGNAL OUTPUT OPTION.
5. E21 & E22 AND/OR E25 & E26 CONNECTED TOGETHER WITHOUT RATIO OPTION.
4. HIGHEST REF DES USED : C19 ; CR13 ; E 27 ; Q 5 ; R13 ; J12 ; S2 ; T1 ; F2
3. ALL VOLTAGES ARE APPROX VALUES MEASURED WITH RESPECT TO ANALOG COMMON.
2. ALL RESISTOR VALUES ARE IN OHMS 1/4 W ± 5% CARBON
1. ALL DIODES ARE SD4

NOTES: UNLESS OTHERWISE SPECIFIED

403081	4530	REF	REF
403185	4570	REF	REF
NEXT DWG	USED ON	NEXT DWG.	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0° 30' FORMED	± .004
XX .020	1° 0'	-.001
XXX .010		

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	J. Tom Gibb	3-27-69
CHECK	V. Graham	4-30-69
DESIGN	Warren Sanborn	4-30-69
MECH ENGR		
PROJ. ENGR	L. Lang	5/1/69
PROD ENGR	W. Gibb	5/6

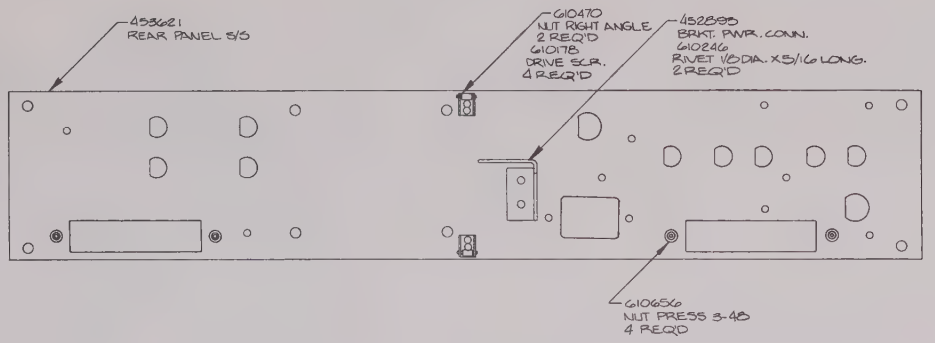
DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

POWER SUPPLY 4500

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430842	D

SCALE | SHEET 1 OF

REVISIONS



1. ASSY. PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403508	5333	1	1
403515	5333	1	1
403527	5333	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	[illegible]	8-19-70
CHECK	Al Godsey	10-AUG 70
DESIGN	H. Hummer	8/9/71
MECH ENGR	[illegible]	8-10-71
PROJ ENGR	K. Yang	8/26/71
PROD ENGR	Revat	8-4-71

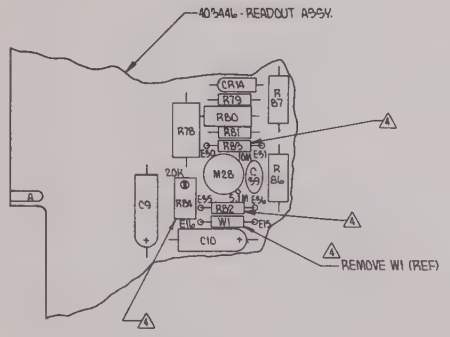
DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

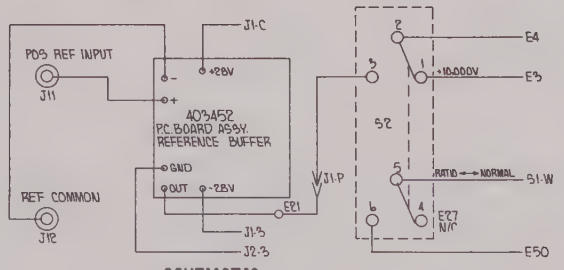
ASSY REAR PANEL

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403509	A

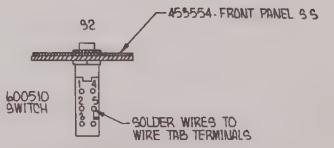
SCALE 1:1 SHEET 1 OF 2

REVISIONS

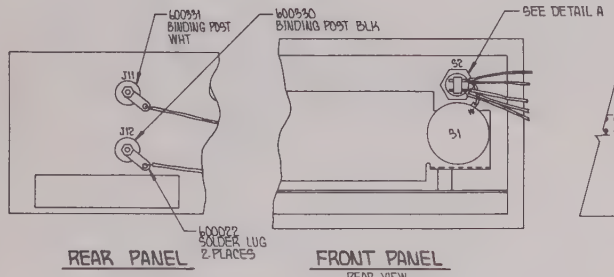




SCHEMATIC

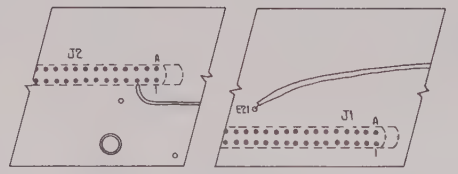


DETAIL A

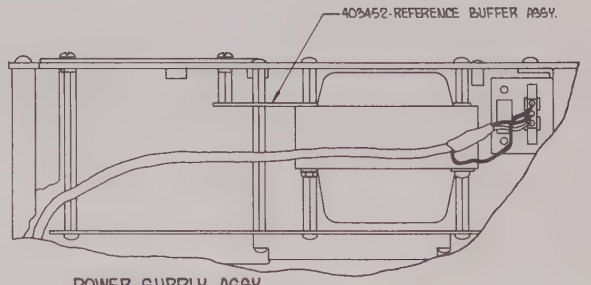


REAR PANEL

FRONT PANEL
REAR VIEW



POWER SUPPLY BOARD
REAR VIEW



POWER SUPPLY ASSY
TOP VIEW

6. SEE NOTE 5 ON 430960 SCHEMATIC FOR RATIO CHANGE.
5. ALL OTHER COMPONENTS ARE FOR REF ONLY.
4. REMOVE JUMPER W1 & ADD RB4 .20K . CHANGE THE VALUES OF RB2 & RB3 TO THOSE SHOWN ON FACE OF DWG.
3. ALL RESISTOR VALUES ARE IN OHMS ±5% 1/4 W. CARBON.
2. SCHEMATIC REF. 430960
1. ASSEMBLY PROCEDURES & PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS.
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
—	5330	—	—
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0° 30'	- .004
XX .020	FORMED	- .001
XXX .010	± 0°	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	Walter M. Haas	7-9-70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	L. Lang	7/16/70
PROD ENGR	D. Pass	7/21

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

RATIO ASSY. 5330
FULL RACK

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403453	A

SCALE 1/1 SHEET 1 OF 2

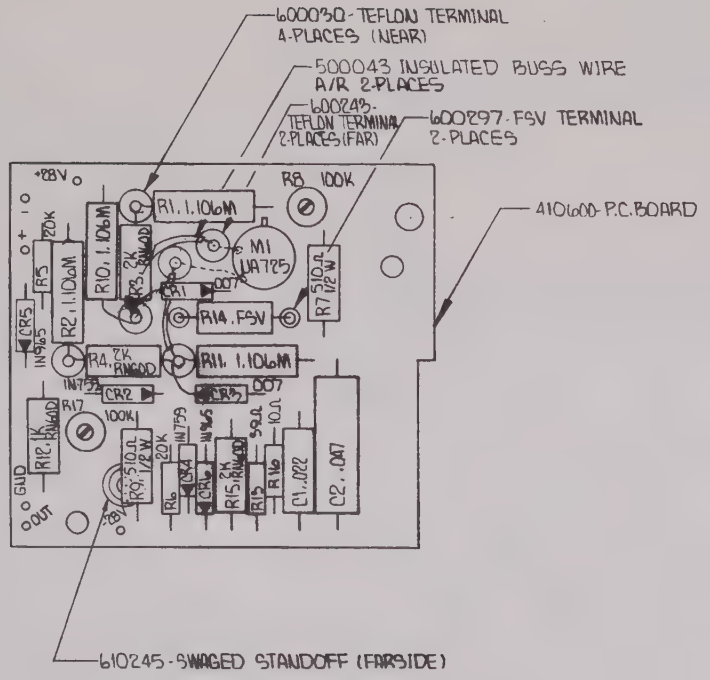
SHEET 2 IS ANSI 'A' SIZE

REVISIONS

This assembly in your instrument may differ from the drawing in the manual. The following information describes differences in alternate revisions of this assembly from that shown. The revision of your assembly is indicated on the circuit board by the letter following the assembly number.

Rev. A

1. Fabrication change only



3. ASSY PROCEDURES AND PROCESSES TO CONFORM WITH DANA WORKMANSHIP STANDARDS.
2. REF. SCHEMATIC 430962.
1. ALL RESISTORS ARE 1/4W ±5% CARBON

NOTES: UNLESS OTHERWISE SPECIFIED

403454	5370	1	1
403452	5330	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Mike McKray	5-1-70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	L Lang	6/8/70
PROD ENGR	D Karp	7/21/70

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C.BOARD ASSY.-
REFERENCE BUFFER

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403452	B

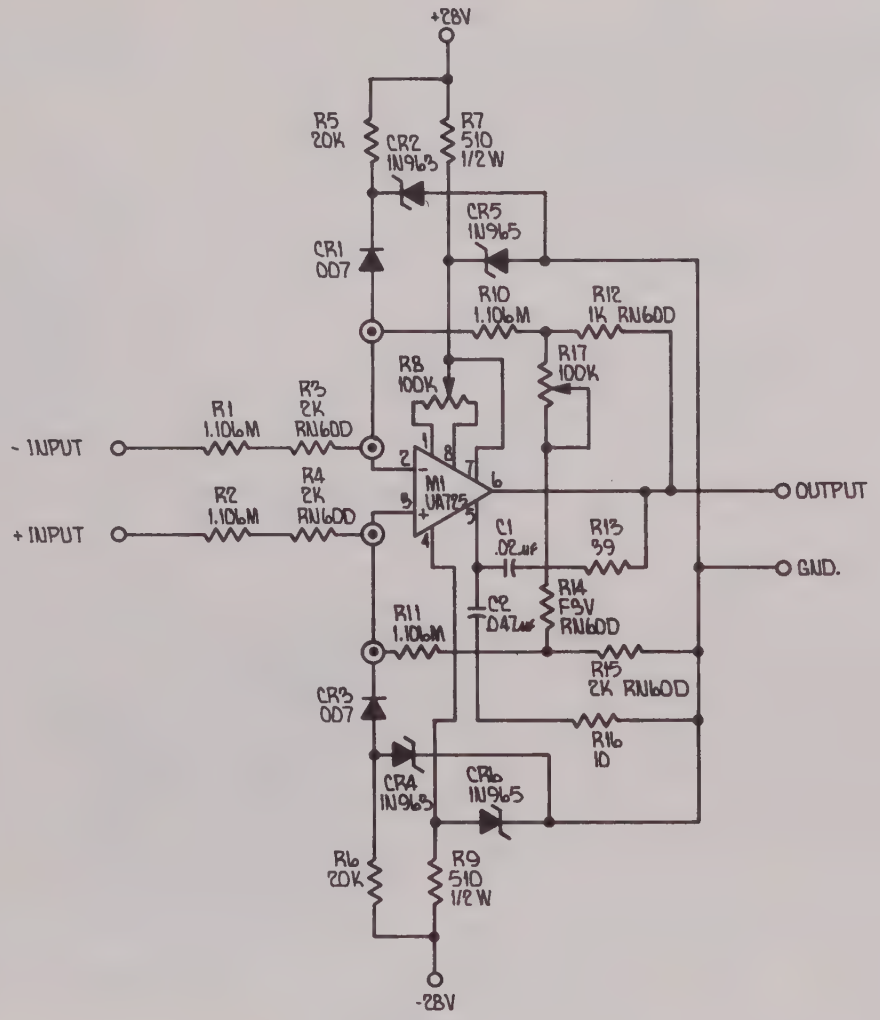
SCALE 2/1 SHEET 1 OF 2

980337 DIETERICH-POST CLEARPRINT 1080

REF 191959-2

SHT 2 - A SIZE

REVISIONS



2. ⊙ INDICATES ISOLATED TERMINAL.
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W ±5% CARBON.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403452	5370	REF	REF
403452	5336	REF	REF
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	Mike McKeay	5-27-70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	L. Long	6/18/70
PROD ENGR	D. Payne	7/21

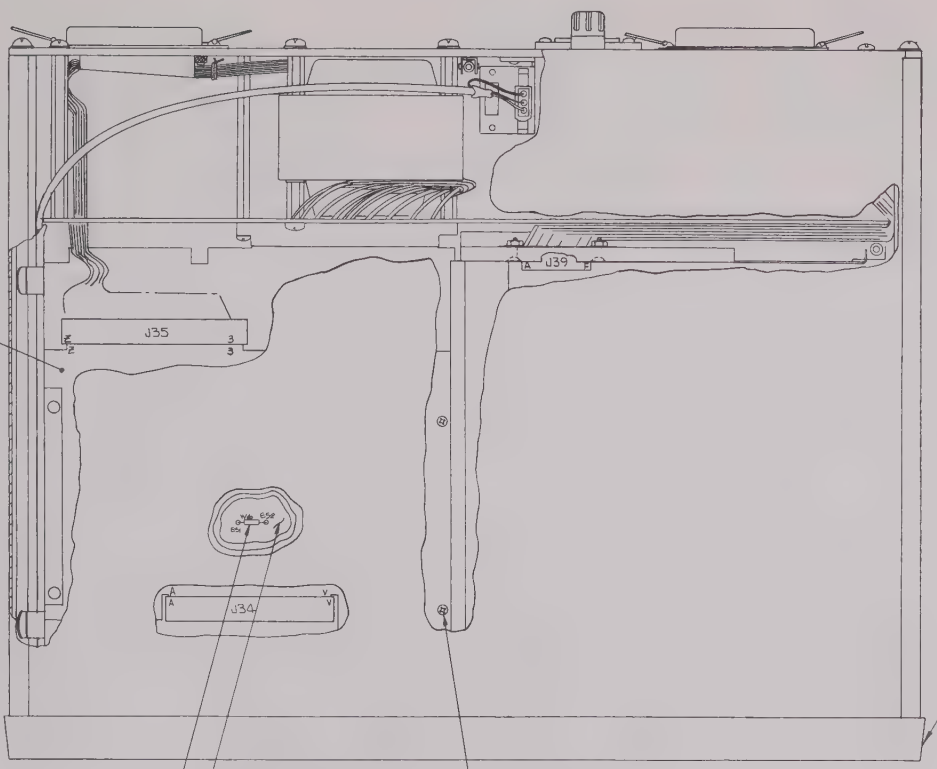
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC - ISOLATOR REFERENCE AND BUFFER

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	430962	A

SCALE ——— SHEET OF

980337 DIETZGEN-POST CLEARPRINT 1080



REVISIONS

⚠ WHEN USED WITH 600 MODULE, ASSY 403551 WILL BE USED.

2. SCHEMATIC REF. #430979

1. ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM WITH DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0° 30'	- .004
XX .020	FORMED	.001
XXX .010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.5

MATERIAL / FINISH

DRAWN		1/25/71	
CHECK			
DESIGN		2/3/71	
MECH ENGR		3-10-71	
PROJ ENGR		3/11/71	
PROD ENGR		3/11/71	

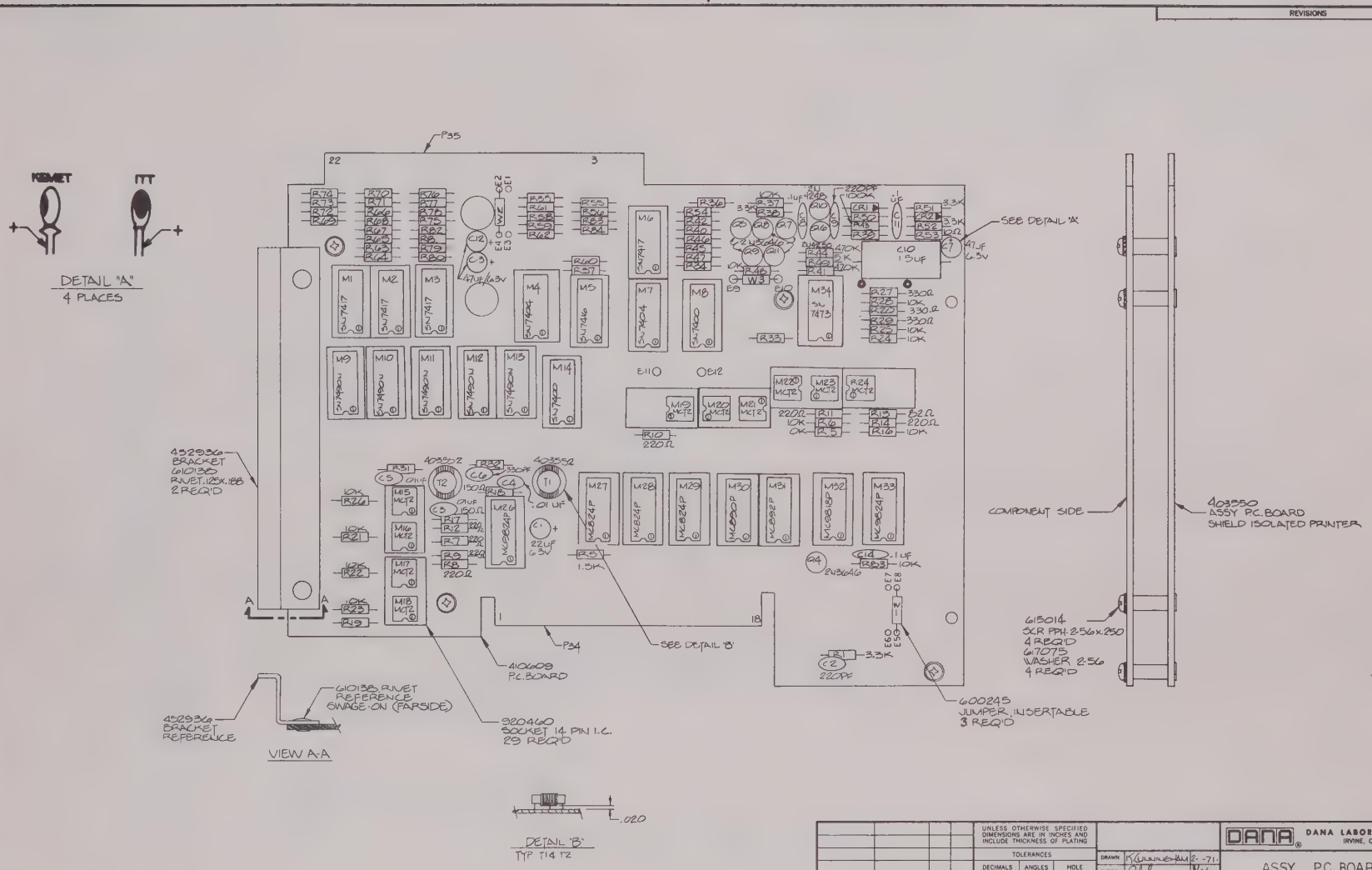
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DVM FULL RACK 5333 ISOLATED PRINTER OUTPUT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	403505	A

SCALE 1:1 SHEET 1 OF 2



4. SCHEMATIC REFERENCE 430979.
3. ALL DIODES 01B'S.
2. ALL RESISTORS 4.7K CARBON 1/4 W ±5%.
1. ASSY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

403505	8333 OPT.		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0° 30'	+ .004
XX .020	FORMED	- .001
XXX .010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

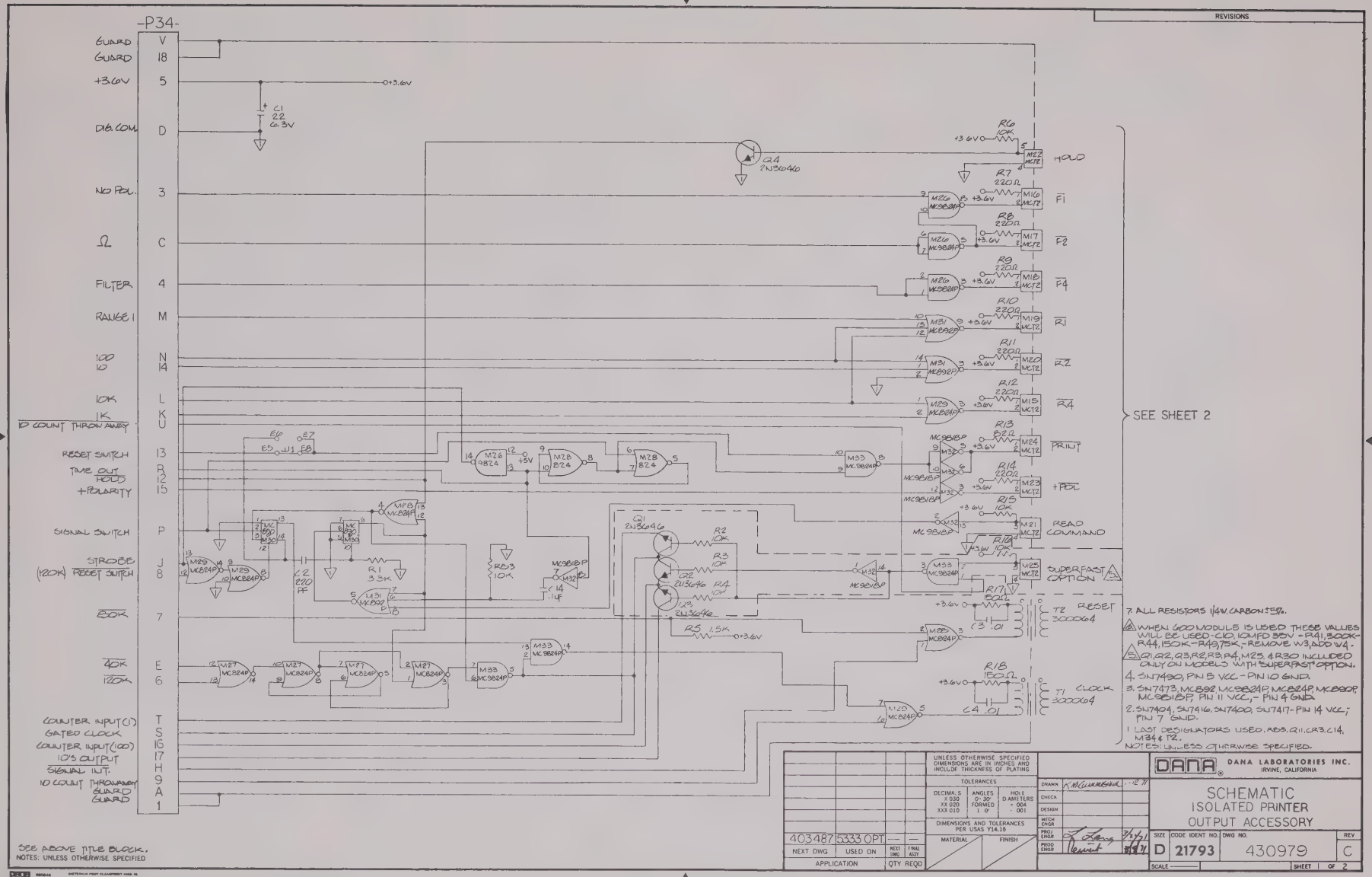
DRAWN	K. Cunningham	2-71
CHECK	[illegible]	3/3/71
DESIGN	K. Cunningham	2-1-71
MECH ENGR		
PROJ ENGR	[signature]	3/1/71
PROD ENGR	[signature]	3/9/71

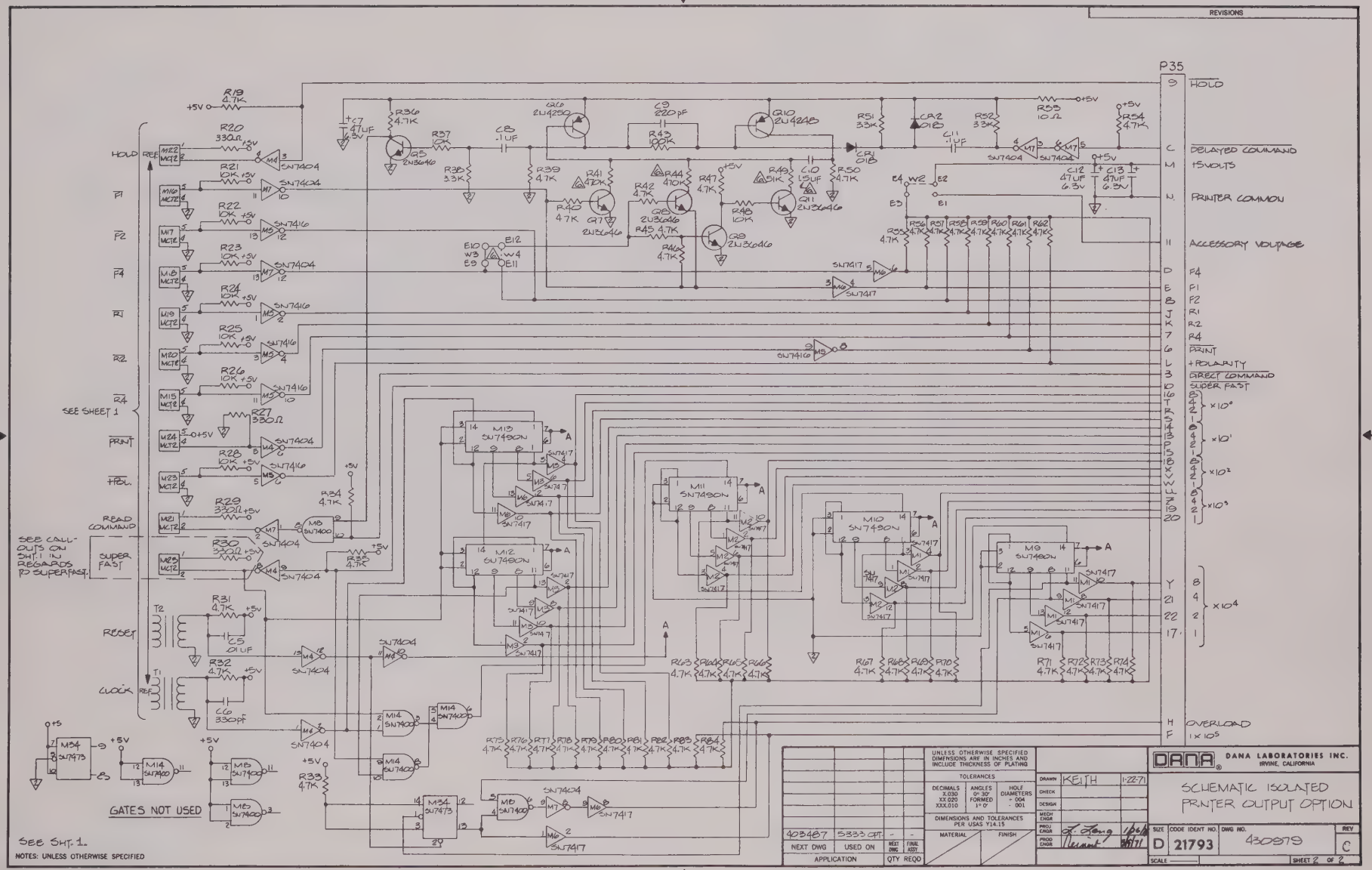
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY P.C. BOARD ISOLATED PRINTER OUTPUT

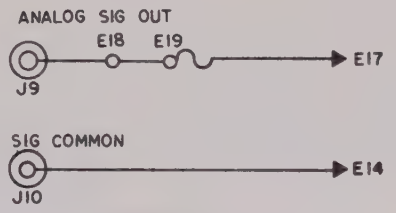
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403487	C

SCALE 2:1 SHEET 1 OF 4


-P34-
GUARD V
GUARD 18
+3.6V 5
DIG. COM. D
NO POL. 3
Ω C
FILTER 4
RANGE 1 M
100 N
10 14
10K L
1K K
10 COUNT THROWAWAY U
RESET SWITCH 13
TIME OUT HOLD 12
+POLARITY 15
SIGNAL SWITCH P
STROBE (120K) RESET SWITCH J
8
120K 7
40K E
120K 6
COUNTER INPUT(1) T
GATED CLOCK S
COUNTER INPUT(100) 16
10'S OUTPUT 17
SIGNAL ILL'T. H
10 COUNT THROWAWAY 9
GUARD A
GUARD 1
C1 22 6.3V
+3.6V
Q4 2N3640
R6 10K
R7 220Ω
R8 220Ω
R9 220Ω
R10 220Ω
R11 220Ω
R12 220Ω
R13 R24
R14 220Ω
R15 10K
R16 10K
R17 150Ω
R18 150Ω
HOLD
F1
F2
F4
R1
R2
R4
PRINT
+POL
READ COMMAND
SUPERFAST OPTION
RESET
CLOCK
C3 .01
C4 .01
T2 3000064
T1 3000064
E8 E7 E5 W1 E8
M26 9824
M28 8T24
M33 MC9824P
MC9818P
M32 MC9818P
M29 MC8824P
M30 MC8824P
M31 MC8824P
M27 MC8824P
M25 MC8824P
M28 MC8824P
M20 MC8824P
M22 MC8824P
M23 MC8824P
M21 MC8824P
M32 MC8824P
M33 MC8824P
M20 MC8824P
M31 MC8824P
M33 MC9824P
M32 MC9818P
M32 MC9818P
M32 MC9818


REVISIONS
P35
HOLD
DELAYED COMMAND
+5VOLTS
PRINTER COMMON
ACCESSORY VOLTAGE
F4
F1
F2
R1
R2
R4
PRINT
+POLARITY
DIRECT COMMAND
SUPER FAST
OVERLOAD
SEE SHEET 1
SEE CALL-OUTS ON SHT. 1 IN REGARDS TO SUPERFAST.
GATES NOT USED
SEE SHT. 1.
NOTES: UNLESS OTHERWISE SPECIFIED
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC ISOLATED PRINTER OUTPUT OPTION
DRAWN KEITH 1-22-71
CODE IDENT NO. 21793
DWG NO. 430979
REV C
SIZE D
SHEET 2 OF 2

WIRING LIST		
FUSE	TO	E NO.
TERM 1		E17
TERM 2		E19
BINDING POST		
JACK	TO	E NO.
J9		E18
J10		E14



SCHEMATIC

REVISIONS

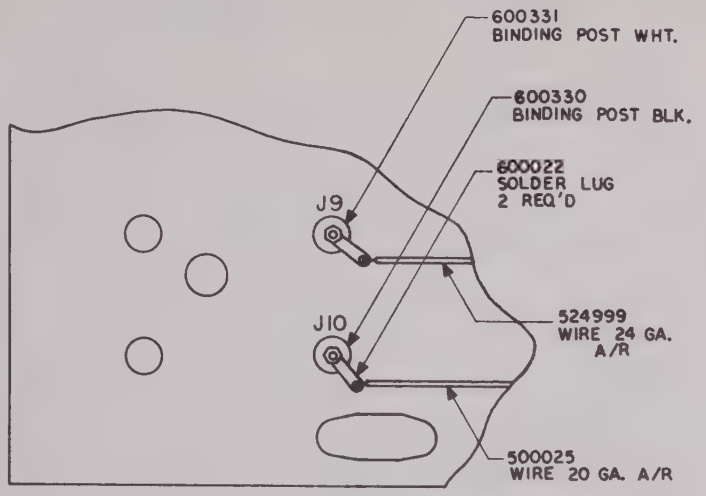
This assembly in your instrument may differ from the drawing in the manual. The following information describes differences in alternate revisions of this assembly from that shown. The revision of your assembly is indicated on the circuit board by the letter following the assembly number.

Rev. B

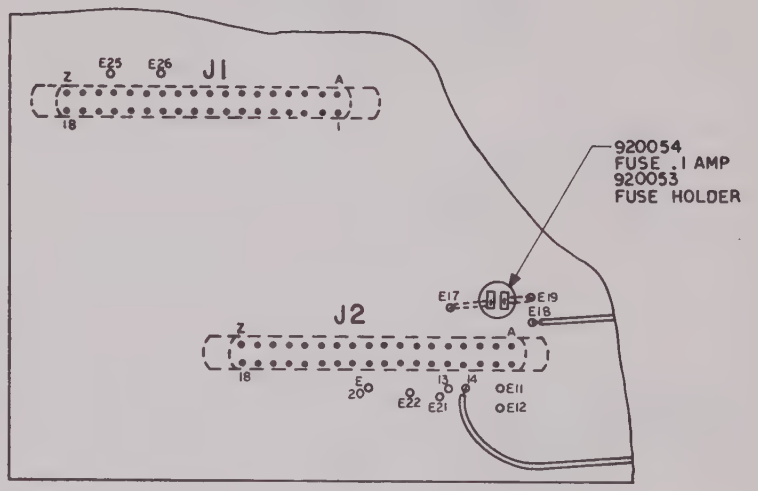
1. On the 5333 J10 is wired to J2-3

Rev. A

1. The change listed for Rev. B (above)
2. Procedure change only



REAR PANEL



POWER SUPPLY BOARD
REAR VIEW

HALF RACK

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	4530		
	4570		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	R. CARROLL	9-19-69
CHECK	W. SARKISON	7-29-69
DESIGN	P. GUMMESON	7-29-69
MECH ENGR		
PROJ ENGR	W. SARKISON	7-30-69
PROD ENGR	P. SALERNO	7-31-69

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY ANALOG SIGNAL OUTPUT

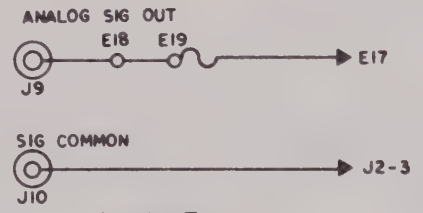
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403262	C

SCALE — SHEET 1 OF 3

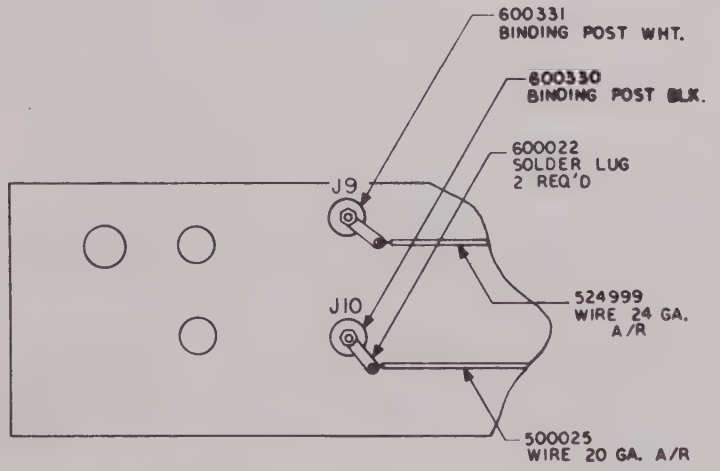
DANA 980337 DIETERICH-POST CLEARPRINT 1080

REVISIONS

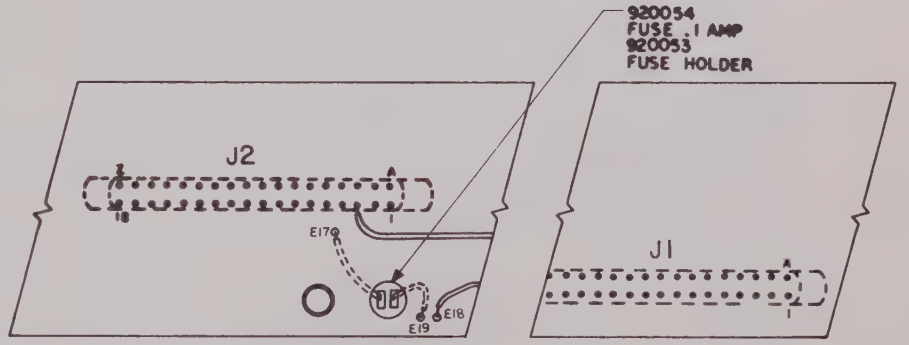
WIRING LIST		
FUSE	TO	E NO.
TERM 1		E17
TERM 2		E19
BINDING POST		
JACK	TO	E NO.
J9		E18
J10		J2-3



SCHEMATIC



REAR PANEL



POWER SUPPLY BOARD
REAR VIEW

FULL RACK

	4530			
	4570			
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30' FORMED 1° 0'	.004 .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	R. CARROLL	9-19-69
CHECK	W. SARKISON	7-29-69
DESIGN	P. GUMMESON	7-29-69
MECH ENGR		
PROJ ENGR	W. SARKISON	7-30-69
PROD ENGR	P. SALERNO	7-31-69

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY ANALOG SIGNAL OUTPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403262	C

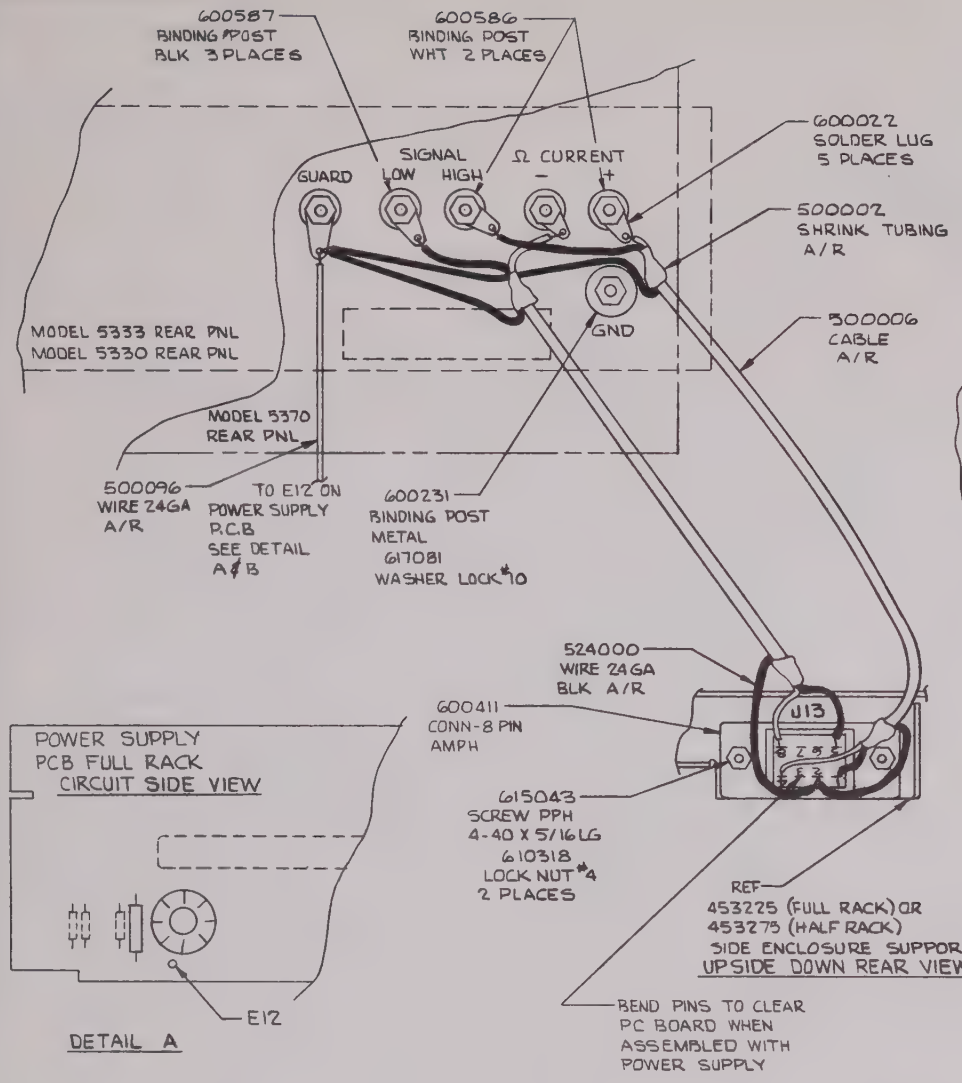
SCALE —— SHEET 2 OF 3

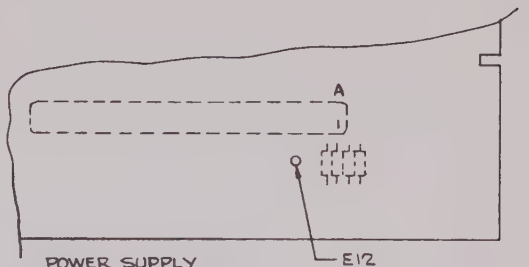
NOTES: UNLESS OTHERWISE SPECIFIED

DANA 980337 DIETERICH-POST CLEARPRINT 1080

This is a A size

REVISIONS

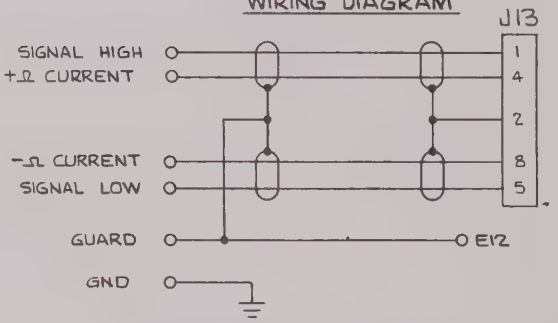




POWER SUPPLY
P.C.B. HALF RACK
CIRCUIT SIDE VIEW
DETAIL B

POWER SUPPLY
PCB FULL RACK
CIRCUIT SIDE VIEW
DETAIL A

WIRING DIAGRAM



—	5333			
—	5300 SER	REF	REF	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	R. Gunnerson	11/20/70
CHECK	Al Godsey	10 MAR 1971
DESIGN	R. Gunnerson	11/20/70
MECH ENGR		3/10/71
PROJ ENGR	L. Lang	3/3/71
PROD ENGR	Reinert	3/8/71

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSEMBLY- REAR INPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403512	A

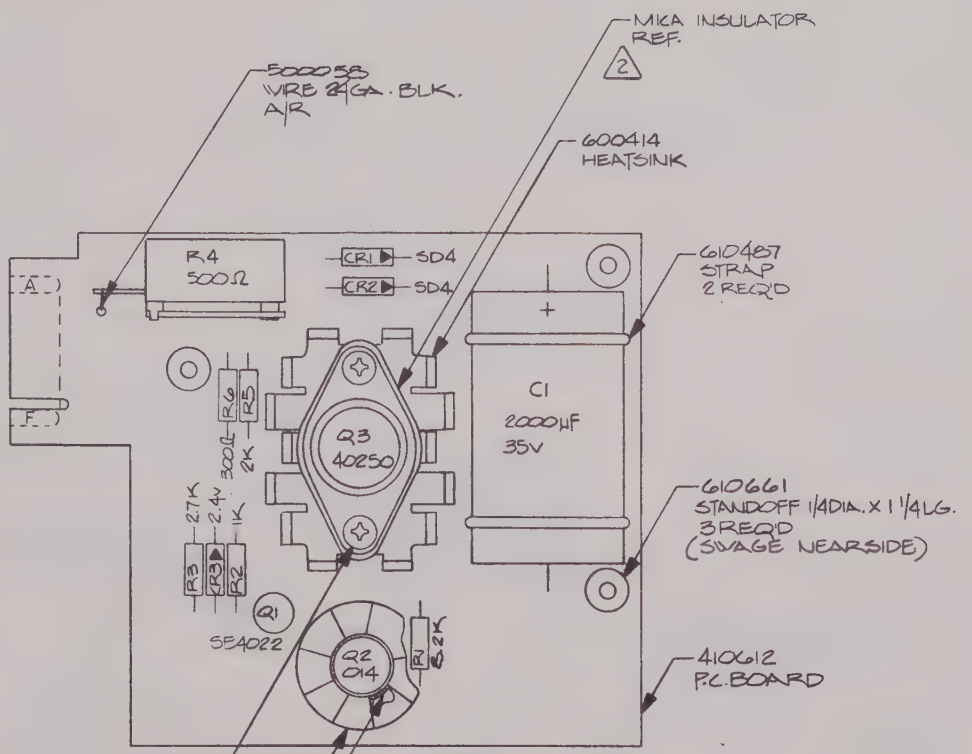
SCALE 1/1 | SHEET 1 OF 2

. DSSY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS

NOTES: UNLESS OTHERWISE SPECIFIED

dana 980337 DIETERICH-POST CLEARPRINT 1020

REVISIONS



3. REF SCHEMATIC NO. 430978.

2. TRANSISTOR IS SUPPLIED WITH MICA WASHER. APPLY SILICONE COMPOUND P/N 920337 TO BOTH SIDES OF OF MICA WASHER.

1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIPS STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403508	5333	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Keith Cummings	DEC 2, 1970
CHECK	A. Hockey	10 MAR 1971
DESIGN	H. Gunnison	2/3/71
MECH ENGR		
PROJ ENGR	T. Tang	2/3/71
PROD ENGR	Clement	3/8/71

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY P.C. BOARD ISOLATED PWR. SUPPLY

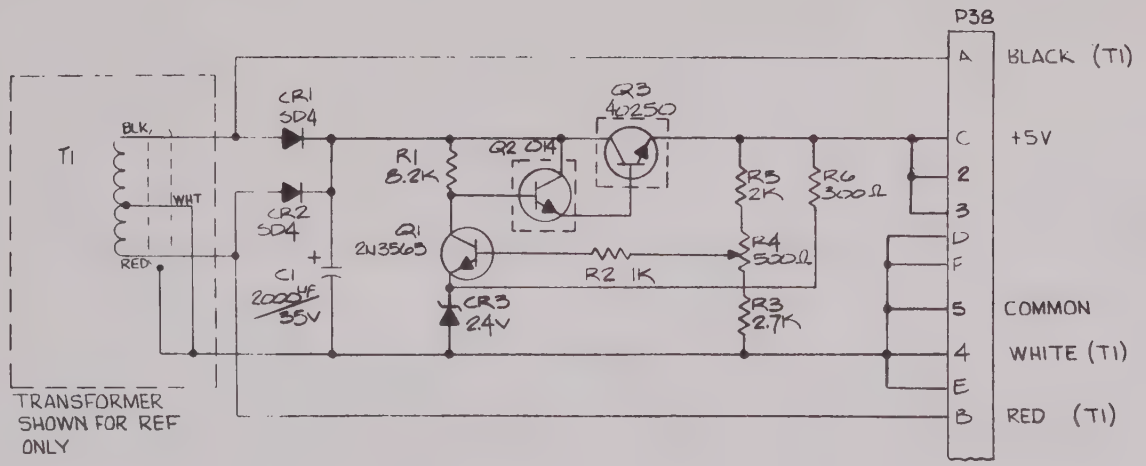
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403495	A

SCALE 2:1 SHEET 1 OF 3

SHEETS 2&3 ARE "A" SIZE

960337 DIETERICH-POST CLEARPRINT 1080

REVISIONS



2. LAST DESIGNATORS USED: CR3, R6, T1, C1, & CR3.
1. ALL RESISTORS 1/4W ±5% C.C.
NOTES: UNLESS OTHERWISE SPECIFIED

403495	5333	REF	REF
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	KEITH CUNNINGHAM	DEC. 16 1970
CHECK	R.C. Mackey	10 MAR 1971
DESIGN		
MECH ENGR		
PROJ ENGR	L. Lang	3/3/71
PROD ENGR	Rivest	3/3/71

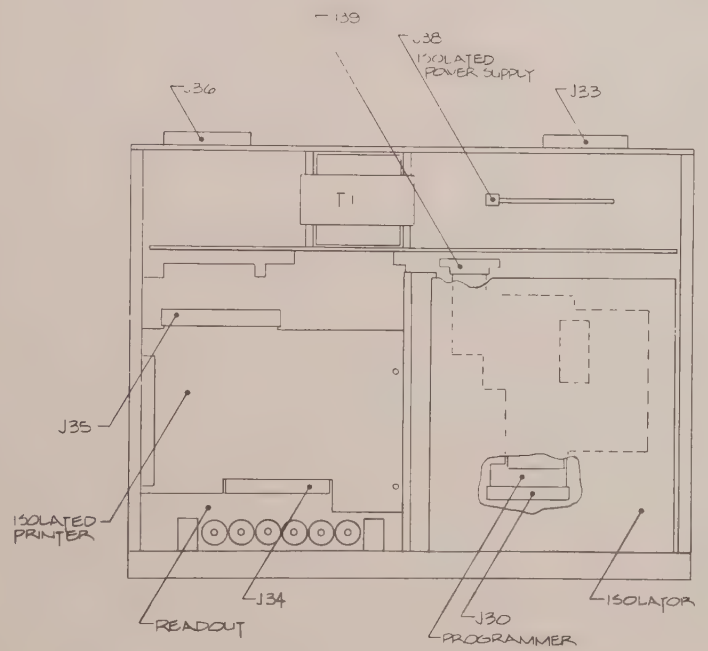
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC ISOLATED POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	430978	A

SCALE NONE | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1001	3/5/71		



READOUT ASSY		J34
GUARD	A	1 GUARD
M9-10	10	3 NO POLARITY
P1-12	B	4 FILTER
+3.6V	U	5 +3.6V
M9-12	7	6 120K
M18-2	13	7 80K
M5-3	4	8 (120K) RESET SWITCH
M7-8	2	9 10 COUNT THROWAWAY
M5-6	H	12 HOLD
M1-13	Z	13 RESET SWITH
P1-17	R	14 10 RANGE
M9-8	L	15 +POLARITY
M12-5	16	16 COUNTER INPUT (100)
M11-2	17	17 10'S OUTPUT
GUARD	V	18 GUARD
GUARD	A	A GUARD
P1-10	9	C Ω
DIGITAL COMMON	11	D DIGITAL COMMON
M18-3	6	E 40K
M9-4	12	H SIGNAL INTEGRATE
M4-5	3	J STROBE
P1-V	P	K 1K RANGE
P1-M	N	L 10K RANGE
P1-U	T	M 1 RANGE
P1-18	5	N 100 RANGE
M3-9	5	P SIGNAL SWITCH
M5-9	Y	R TIME OUT
M4-9	14	S GATED CLOCK
M10-9	15	T COUNTER INPUT (1)
M7-9	K	U 10 COUNT THROWAWAY
GUARD	V	V GUARD

	J35	
DIRECT COMMAND	3	J36-22, J33-23
PRINT	6	J36-42
R4	7	J36-20
F2	8	J36-2
HOLD	9	J36-47 / J33-47
SUPERFAST	10	J36-49 / J33-49
ACCESSORY VOLTS	11	J36-25
4x10¹	13	J36-32
8x10¹	14	J36-33
1x10¹	15	J36-7
8x10⁰	16	J36-3
1x10⁴	17	J36-3
8x10²	18	J36-35
2x10³	19	J36-12
1x10³	20	J36-11
4x10⁴	21	J36-38
2x10⁴	22	J36-4
DELAYED COMMAND	C	J36-22 / J33-22
F4	D	J36-42
F1	E	J36-17
1x10⁵	F	J36-5
OVERLOAD	H	J36-21
R1	J	J36-1
R2	K	J36-2
+POLARITY	L	J36-3
+5VOLTS	M	J36-3
PRINTER COMMON	N	J36-E
2x10¹	P	J36-8
2x10⁰	R	J36-6
1x10⁰	S	J36-5
4x10⁰	T	J36-30
8x10³	U	J36-37
2x10²	V	J36-10
1x10²	W	J36-9
4x10²	X	J36-34
8x10⁴	Y	J36-39
4x10³	Z	J36-36
NO CONNECTION	1	
	2	
	4	
	5	
	12	
	A	
	B	

	J30	
R1	1	J35-N
R2	2	J35-A
+POLARITY	3	J35-L
COMMON	4	
1x10⁰	5	J35-S
2x10⁰	6	J35-R
1x10	7	J35-15
2x10¹	8	J35-P
1x10²	9	J35-W
2x10²	10	J35-V
1x10³	11	J35-20
2x10³	12	J35-19
1x10⁴	13	J35-17
2x10⁴	14	J35-22
1x10⁵	15	J35-F
2x10⁵	16	J36-24
F1	17	J35-E
F2	18	J35-B
OVERLOAD	21	J35-H
DELAYED COMMAND	22	J35-C
DIRECT COMMAND	23	J35-3
PRINTER COMMON	24	J35-F
ACCESSORY VOLTS	25	J35-11
R4	26	J35-7
R8	27	J36-24
COMMON	28	
COMMON	29	
4x10⁰	30	J35-T
8x10⁰	31	J35-16
4x10¹	32	J35-13
8x10¹	33	J35-14
4x10²	34	J35-X
8x10²	35	J35-18
4x10³	36	J35-Z
8x10³	37	J35-U
4x10⁴	38	J35-21
8x10⁴	39	J35-Y
4x10⁵	40	J36-24
8x10⁵	41	J36-24
F4	42	J35-D
HOLD	47	J35-9
PRINT	48	J35-6
SUPERFAST	49	J35-10
+5 VOLTS	50	J35-2
F8	43	
NO CONNECTION	44	
	45	
	46	

NOTES: UNLESS OTHERWISE SPECIFIED

	5333	—	—	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	K CUNNINGHAM	2-9-71
CHECK	T. Kang	3/5/71
DESIGN	V. Gamma	3/4/71
MECH ENGR		
PROJ ENGR	T. Kang	3/5/71
PROD ENGR	Vincent	3/9/71

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC INTERCONNECTION

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430983	A

SCALE 1/2 SHEET 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
—	RELEASED PER DRN # SEE SHEET 1			

J37

R	1	J39-E
R2	2	J39-L
F	4	J39-
F2	5	J39-2
FR	7	E13(RATIO OPTION)
DELAYED COMMAND	22	J35-C
DIRECT COMMAND	23	J35-B
PROGRAM COMMON	24	J38-F
R4	26	J39-C
F4	29	J39-B
REMOTE	37	J39-F
HOLD	47	J35-9
SUPERFAST	48	J35-10
+5 VOLTS	50	J38-2
NO CONNECTION	3, 7, 8, 9, 10, 12, 13, 14, 15, 16, 20, 21, 25, 27, 28, 30, 31, 32, 33, 34, 35, 36, 38, 39, 40, 41, 42, 43, 44, 45, 46, 49	

J38

+5 VOLTS	2	J33-5C/J36-50
+5 VOLTS	3	J35-M
	A	T1 (BLACK)
	B	T1 (RED)
+5 VOLTS	C	J39-4
COMMON	D	J38-3
COMMON	E	J35-N
COMMON	F	J33-24/J36-24
COMMON	4	T1 (WHITE
SHIELD	5	J38-E
NO CONNECTION	1, 6	

T1

BLK	J38-A
RED	J38-B
WHT	PRINTER COMMON J38-D

J39

F1	1	J33-4
F2	2	J33-5
PROGRAM COMMON	3	J38-D
+5 VOLTS	4	J38-C
F4	B	J33-29
R4	C	J33-26
R2	D	J33-2
R1	E	J33-1
REMOTE	F	J35-37
NO CONNECTION	5, 6, A	

J30

DIGITAL COMMON	2	1	DIGITAL COMMON
K FILTER	3	1	K4-1
K A.C.	4		K5-1
K OHMS	5		K6-1
FILTER	6		S11-16
REMOTE LAMP	7		S1 FRONT PANEL (SEE 403504)
+28 VOLTS	8	12	+28 VOLTS
R1	11		S4-3
R2	12		S4-4
R3	13		S8-6
R3	14		S8-4
R2	15		S7-6
R1	16		S5-3
AUTO RANGE	17		S10-4
REMOTE	18	6	
GUARD	A		GUARD - FRONT PANEL
+3.6 VOLTS	B	2	+3.6 VOLTS
OHMS	C		S3-13
A.C.	D		S2-7
.1 RANGE	E		S2-12
RESET R1	F	E4	M12-12
10K RANGE	H		S3-10
OHMS	J		S3-15
D.C.	K		S1-6
A.C.	L		S2-9
(GROUND)(REMOTE)	M		S10-5
(R2)(AUTO)	N		S10-8
COMMON AUTO	P		S10-2
COMMON FILTER	R		S11-11
COMMON D.C.	S		S1-2
COMMON A.C.	T		S2-10
COMMON RANGE	U		S9-2
COMMON OHMS	V		S3-14
NO CONNECTION	1, 9, 10		

SEE SHEET 1.

NOTES: UNLESS OTHERWISE SPECIFIED

	5333			
NEXT DWG	USED ON	NEXT ASSY	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+ .004
XX.020	FORMED	- .001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN		2-9-71
CHECK		3/2/71
DESIGN		3/2/71
MECH ENGR		
PROJ ENGR		3/2/71
PROD ENGR		3/6/71

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC INTERCONNECTION

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430983	A

SCALE —— SHEET 2 OF 2

PARTS LIST

ASSEMBLY 403081 - Model 5333 A

REF. DESIG.	PART NO.	DESCRIPTION							
CR01	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR02	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR03	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR04	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR05	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR06	210004	DIODE SILICO	SD4				DIODES IN SD4		
CR07	210014	DIODE SILICO	023				DANA	210014	
CR08	210014	DIODE SILICO	023				DANA	210014	
CR09	210014	DIODE SILICO	023				DANA	210014	
CR10	210014	DIODE SILICO	023				DANA	210014	
CR11	221177	DIODE SILICO ZENER			1/4 W		MOTOROLA	M.2.4A25	
CR12	220035	DIODE ZENER	IN966B				MOTOROLA	IN966B	
CR13	220035	DIODE ZENER	IN966B				MOTOROLA	IN966B	
C02	121088	CAP MYLAR	.01	MFD	100 V	10%	CDE	WMF1S1	
C03	121088	CAP MYLAR	.01	MFD	100 V	10%	CDE	WMF1S1	
C04	120072	CAP MYLAR	.01	MFD	600 V	10%	CDE	WMF651	
C05	110067	CAP ELECT	2000	MFD	35 V	20%	DUCATI	2000-35	
C06	110107	CAP ELECT	4000	MFD	15 V		DUCATI	4000DX1512-10	
C07	110065	CAP ELECT	20	MFD	350 V	20%	DUCATI	20-350	
C08	110067	CAP ELECT	2000	MFD	35 V	20%	DUCATI	2000-35	
C09	120003	CAP MYLAR	.1	MFD	100 V	10%	CDE	WMF1P1	
C10	120003	CAP MYLAR	.1	MFD	100 V	10%	CDE	WMF1P1	
C11	110066	CAP ELECT	15	MFD	200 V	20%	DUCATI	15-200	
C12	110070	CAP ELECT	22	MFD	6 V	10%	KEMET	K22W6K	
C13	100017	CAP CERAM	.01	MFD	200 V	10%	SPRAGUE	TH-S10	
C14	110043	CAP ELECT	25	MFD	25 V	20%	DUCATI	25-25	
C15	110043	CAP ELECT	25	MFD	25 V	20%	DUCATI	25-25	
C16	101174	CAP CERAM	.001	MFD	500 V	10%	AEROVOX	SCD3X5F	
C17	101174	CAP CERAM	.001	MFD	500 V	10%	AEROVOX	SCD3X5F	
C18	110077	CAP ELECT	1000	MFD	15 V		AMPEREX	C437PR/E1000	
C19	120019	CAP MYLAR	.47	MFD	100 V	10%	CDE	WMF1P47	
Q01	200043	TRANS SILICO NPN	2N3565				FAIRCHILD	2N3565	
Q02	200035	TRANS SILICO NPN	014				DANA	200035	
Q03	200030	TRANS SILICO NPN	40250				RCA	40250	
Q04	200035	TRANS SILICO NPN	014				DANA	200035	
Q05	200052	TRANS SILICO PNP	009				DANA	200052	

PARTS LIST

ASSEMBLY 403081 - Model 5333 A

REF. DESIG.	PART NO.	DESCRIPTION							
R01	000224	RES	CARBON	220	K	5%	1/4 W	OHMITE	RC07GF224J
R02	030014	RES	CARBON	220	K	5%	1 W	OHMITE	RC32GF224J
R03	000472	RES	CARBON	4.7	K	5%	1/4 W	OHMITE	RC07GF472J
R04	000101	RES	CARBON	100	OHM	5%	1/4 W	OHMITE	RC07GF101J
R05	000102	RES	CARBON	1	K	5%	1/4 W	OHMITE	RC07GF102J
R06	000102	RES	CARBON	1	K	5%	1/4 W	OHMITE	RC07GF102J
R07	000202	RES	CARBON	2	K	5%	1/4 W	OHMITE	RC07GF202J
R08	040063	RES	VARI	500	OHM	10%	1.5 W	CTS	110
R09	000511	RES	CARBON	510	OHM	5%	1/4 W	OHMITE	RC07GF511J
R10	000151	RES	CARBON	150	OHM	5%	1/4 W	OHMITE	RC07GF151J
R11	000151	RES	CARBON	150	OHM	5%	1/4 W	OHMITE	RC07GF151J
R12	030007	RES	CARBON	150	OHM	5%	3 W	OHMITE	4396
R13	030007	RES	CARBON	150	OHM	5%	3 W	OHMITE	4396

PARTS LIST

ASSEMBLY 403453 - Model 5333 A

REF. DESIG.	PART NO.	DESCRIPTION							
R82	000515	RES	CARBON	5.1 M	5%	1/4 W	OHMITE	RC07GF515J	
R83	000106	RES	CARBON	10 M	5%	1/4 W	OHMITE	RC07GF106J	
R84	040092	RES	VARI	20 K			SPECTRO	50-3-1-203	

PARTS LIST

ASSEMBLY 403452 - Model 5333 A

REF. DESIG.	PART NO.	DESCRIPTION							
CR01	211236	DIODE SILICO	007					DANA	211236
CR02	220029	DIODE ZENER						MOTOROLA	1N759A
CR03	211236	DIODE SILICO	007					DANA	211236
CR04	220029	DIODE ZENER						MOTOROLA	1N759A
CR05	220022	DIODE SILICO ZENER 1N965B						MOTOROLA	1N965B
CR06	220022	DIODE SILICO ZENER 1N965B						MOTOROLA	1N965B
C01	121468	CAP MYLAR	.022 MFD 100 V			10%		CDE	WMF1S22
C02	121093	CAP MYLAR	.047 MFD 100 V			10%		CDE	WMF1S47
M01	230070	INTEGRATED CIRCUIT	UA725					FAIRCHILD	U5B7725393
R01	010465	RES METAL	1.106 MEG			.1%		PYROFILM	PME 65-T9
R02	010465	RES METAL	1.106 MEG			.1%		PYROFILM	PME 65-T9
R05	000203	RES CARBON	20 K		5%	1/4 W		OHMITE	RC07GF203J
R06	000203	RES CARBON	20 K		5%	1/4 W		OHMITE	RC07GF203J
R07	001706	RES CARBON	510 OHM		5%	1/2 W		OHMITE	RC20GF511J
R08	040088	RES VARI	100 K		10%			BECKMAN	62PR100K
R09	001706	RES CARBON	510 OHM		5%	1/2 W		OHMITE	RC20GF511J
R10	010465	RES METAL	1.106 MEG		.1%			PYROFILM	PME 65-T9
R11	010465	RES METAL	1.106 MEG		.1%			PYROFILM	PME 65-T9
R12	010347	RES METAL	2 K		1%			IRC	RN60D
R13	000390	RES CARBON	39 OHM		5%	1/4 W		OHMITE	RC07GF390J
R14		RES FSV			1%			IRC	RN60D
R15	010347	RES METAL	2 K		1%			IRC	RN60D
R16	000100	RES CARBON	10 OHM		5%	1/4 W		OHMITE	RC07GF100J
R17	040088	RES VARI	100 K		10%			BECKMAN	62PR100K

DANA.

MP MASTER
MA30565